An integrated radar tile for Digital Beam Forming X/Ka band Synthetic Aperture Radar Instruments

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***Abstract*—This work presents the first experimental assessment of a highly integrated dual-band dual-polarized antenna tile designed for Synthetic Aperture Radar (SAR) Digital Beam Forming (DBF) satellite applications. The demonstrator described in this paper is the first comprehensive experimental validation of an RF module providing X- and Ka-band (9.6 and 35.75 GHz) operation with custom down-conversion stages. All the antennas, transitions and down-conversion chips are integrated in the same antenna tile fabricated using a customized 15-layer High Density Interconnect (HDI) process. The designed tile goes to the limits of the proposed technology and for the high trace density and for the size of the vertical transitions. The proposed results represent the state of the art in terms of compactness for a DBF SAR RF module even though the demonstrator was manufactured with a standard low cost technology. The experimental assessment proves the validity of the proposed manufacturing and integration approaches showing a substantial agreement between the performance of the individual blocks and of the integrated system.**

***Index Terms*—Synthetic aperture radar, digital beam forming, antenna, integrated systems, small satellite**

I. Introduction

Earth observation (EO) is one of the fastest growing sectors in the space market [1]. Main growth drivers for EO data and services are not limited to defense and security applications but include also mapping of infrastructure and natural resources, monitoring and responding to natural disasters, addressing public health and maritime safety. New applications are constantly developed requiring competitively-priced technological solutions which should lower the cost of both sensors and satellite platforms while providing increased sensitivity, resolution and coverage. In this perspective, small satellites represent a relevant opportunity that is being undertaken by several satellite operators. However, even though optical sensors can be easily integrated in cube-sats, the use of Synthetic Aperture Radars (SAR) has been typically precluded to small satellite platforms due to the inherent volume and mass limitations. Recently [2], it has been demonstrated how high-resolution wide-swath SAR imaging

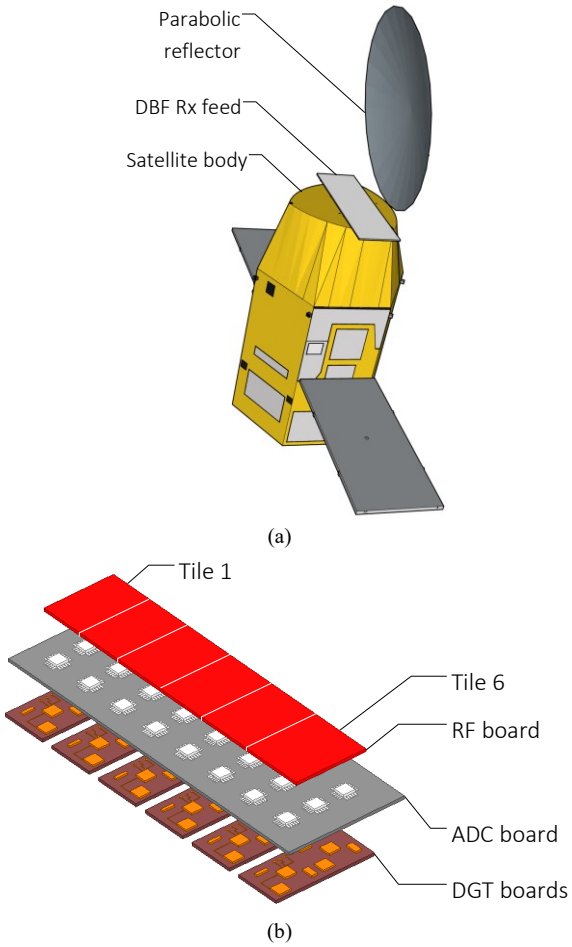


Fig. 1 Digital beamforming synthetic aperture radar (SAR) architecture: a) pictorial view of the DBF Rx SAR instrument integrated on a satellite; b) tile based architecture of the DBF Rx SAR feed.

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sensors could be designed employing Digital Beam Forming (DBF) techniques in a receive-only multistatic satellite constellation. The introduction of these architectures allows the development of new SAR systems where a single master satellite illuminates the Earth surface and a constellation of small satellites equipped with compact DBF SAR sensors scans the scattered field following the echo on ground [3]. The implementation of this new architecture relies on the possibility to exploit highly integrated DBF SAR sensors. However, existing DBF SAR spaceborne instruments do not match these compactness and modularity requirements [4]. Several concurrent research activities are tackling the development of compact DBF SAR sensors proposing different solutions. For example, in [5] it is presented a three-channel DBF SAR antenna providing dual-polarized L-band operation. This system uses a hybrid analog/digital beam-forming scheme where groups of four sub-arrays share the same digital channel. Another possible implementation is being developed within the framework of the EU project [6]. The challenge of this project is to implement a receive-only SAR sensor capable to acquire data in two bands, namely in X and Ka band, in single-pass full polarimetric mode. The adopted center-band frequencies in X- and Ka-band are 9.6 and 35.75 GHz, respectively. In the proposed architecture, a DBF feed array with 60 digital channels is used to illuminate a deployable reflector [7], [8] as shown in Fig. 1-a. High resolution is achieved combining the benefits of the multistatic constellation with the multichannel capability enabled by the DBF technique and with the dual-band single-pass full polarimetric acquisitions [9]. Moreover, the flexibility of this SAR receiver platform will support the realization of a variety of spaceborne SAR missions [10].

The feasibility of this approach relies on the capability to realize a highly integrated and modular DBF reflector feed. The required compactness is reached distributing the different components into three boards named: i) RF board; ii) ADC board and iii) DGT board. The basic design principles underpinning the adoption of the proposed configuration are described in [6] where the simulated and measured results of the isolated subsystems of the RF board are also presented. This paper expands upon the previous work by providing an extensive report on the integration strategy along with detailed numerical and experimental assessment of a fully assembled RF-board tile. This paper is organized as follows. Section II describes the architecture of the SAR instrument. Section III illustrates the integration strategy and the board stack-up. Section IV and V present the configuration and the integration of the MMICs and of the antennas, respectively, while Section VI describes the most critical manufacturing issues. Finally, measured results are presented in Section VII.

II. SAR INSTRUMENT ARCHITECTURE

The architecture of the proposed SAR instrument, shown in Fig. 1-b, is designed to guarantee a modular approach easily adaptable to different mission contexts. One of the fundamental building blocks is the antenna tile which embeds dual-band dual-polarized array cells and the microwave monolithically integrated chips (MMIC) which operate the down conversion

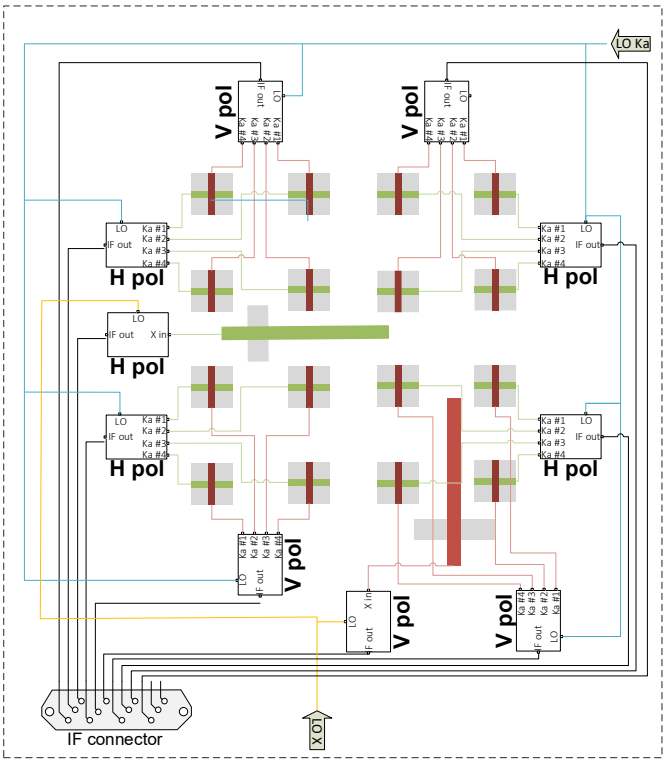


Fig. 2 Architecture of the single radar tile.

of the RF signal to an intermediate frequency (IF). Combinations of tiles constitute the RF-board which can be used to form a feed array reflector [11]. As shown in Fig. 2, each tile is a self-consistent module providing 10 IF output channels, 8 in Ka and 2 in X band. It accommodates:

- 1 H-polarized X-band antenna;
- 1 V-polarized X-band antenna;
- 16 Ka-band dual-polarized antennas arranged in sub-arrays of 4 elements;
- 2 MMIC chips at X band (for V and H polarized signals);
- 8 MMIC chips at Ka band (4 for V and 4 for H polarized signals);
- 2 Local Oscillator (LO) distribution networks for the two bands (X and Ka).

The function of the chips is to amplify and down-convert the received V- and H-pol signals to an Intermediate Frequency (IF). For the case at hand, two types of MMICs are employed. Hence, each X-band antenna is connected to a single-channel MMIC while the signal received by each 2x2 sub-array of Ka-band elements in a single polarization is power combined and down-converted using a dedicated chip. The IF signals generated by each chip are routed, through an output IF connector, to the ADC board where they are digitalized. Finally, the digital data corresponding to each polarization and to each radiating element are weighted and combined in the digital beam forming network (DBFN) implemented using six digital boards. The electrical connection between the boards shown in Fig.1-b(b)

Fig. 1 is ensured by special connectors that allow a simple mounting/dismounting of the modules also during the assembly and testing phases. This approach is extremely important to experimentally assess the final demonstrator which embodies 6 tiles (Fig. 1-b) and 60 digital channels.

III. STACK-UP VERTICAL DESIGN AND KEY BUILDING BLOCKS

This paper describes the design, manufacturing and experimental validation of a single radar tile demonstrating the correct operation of the sub-system composed by several components integrated in a single board. The radiating elements, RF circuits and MIMCs are embedded on the same multilayer printed circuit board (PCB) to reduce the complexity of the system obtaining an extremely compact component. In general, the required high density of the manifold could be implemented using low-temperature cofired ceramics (LTCC) [12] that can guarantee low loss and a variety of vertical transitions. However, this technology is costly and manufacturing reliability can not be guaranteed over large areas [13]. For this reason, in this work the challenge was to design a highly dense PCB using a standard industrial process yet guaranteeing the required level of density and limiting the losses. A first example of complex stack-up for this application was presented in [6]. However, this configuration allows only the integration of a subset of the tile components. In this work, the previously presented buildup is simplified with the objective to reduce the manufacturing complexity and costs while guaranteeing the full tile integration. This goal has been achieved through the minimization of the layers' number, of the blind and buried vertical interconnect access (via) typologies, and of vias aspect ratio. However, although the reduction of the fabrication steps limits the manufacturing cost it has a direct impact on the electromagnetic performance of all the integrated components thus requiring a trade-off between technological constraints and electromagnetic requirements. Details about this optimization process are given in Section III-A which describes the solutions employed to design the antennas and their vertical transitions using a simplified buildup.

Fig. 3 shows the proposed stack-up used to design the radar tile where black areas refer to metallization, dark grey areas refer to dielectric substrate, light grey areas refers to foam spacers and black circles correspond to metallized vias passing through the layers. The technology used in this work is based on an advanced multilayer PCB technology, which includes 15 layers of metallization. Cavities are carved between layers L1 and L3 to accommodate the MMIC chips. Layers between L9 and L15 have been used to integrate the antennas (see Section V). Layers L6 and L7 are employed to route the six output IF channels and to provide power distribution between the integrated chips. Layer L4 implements two local oscillator (LO) distribution networks for the X- and Ka-band (see Section IV.A). Layer L1 is used to route the IF signals generated by each chip (see Sections III-0, IV and V-**Errore. L'origine riferimento non è stata trovata.**) and for the integration of input and output connectors.

With respect to the stack-up model employed in [6], in the one here proposed the types of vias are reduced from 4 to 2, namely:

- Type#1: from L1 to L11;
- Type#2: from L1 to L5.

In fact, when necessary, back drilling is used to remove the lower part of type #1 via (as shown in Fig. 3) to allow connection also from L1 to L9 and L10. Back drilling is a

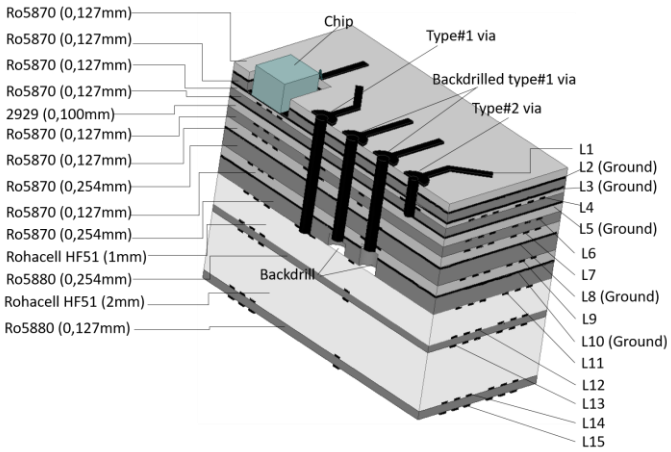


Fig. 3 Stack-up employed to design the proposed RF board tile. The figure shows the 15 copper layers (L1, L2, … ,L15) and the dielectric cores. A special fabrication procedure has been used to avoid the use of prepreg between core layers.

controlled depth drilling technique that removes part of the via with conventional numerically controlled drill equipment. As a further simplification, the proposed stack-up has been manufactured using a fusion technique which allows to bond the core layers without using prepregs. In this way a more homogeneous layup, without unwanted dielectric constant variations in the vertical direction, is available for the integration of the high frequency antennas and transmission striplines. This technique also reduces the roughness of the printed striplines as all the metal layers can be based on rolled copper. For the case at hand, core layers are based on Rogers Ro5870 and Ro5880 substrates. These materials present relative dielectric permittivity of 2.33 and 2.2, respectively, while the loss tangent are equal to 0.0012 and 0.0009, respectively.

A. Analysis and simplification of the vertical interconnections

One of the most critical components in the design of the RF board tile is the vertical transition between antennas and chips which are placed on the opposite sides of the stack-up. To avoid high insertion losses, these interconnections were realized using a quasi-coaxial configuration [14], [15] where a central signal via is surrounded by a number of ground vias (see image inside Fig. 4). Ground vias form an outer conductive boundary within which the field configuration is similar to that of a coaxial transmission line. A first estimation of the characteristic impedance can be obtained using the analytical equations of an ideal coaxial line having continuous conductive boundaries. However, metallized via-holes and their associated pads constitute a relevant geometrical inhomogeneity which has to be evaluated through full-wave simulations.

In the proposed configuration, two types of interconnections are required between the 50-ohm microstrip lines on L1 and the X- and Ka-band antennas whose feed lines are located on L11 and L9, respectively. In order to simplify the stack-up, both transitions were realized employing a single via type, namely Type#1. However, although this solution does not pose any issue in the case of interconnection between L1 and L11, it can be critical for the transition between Ka-antennas on L9 and the MMICs on L1. Indeed, in the latter case a portion of signal via

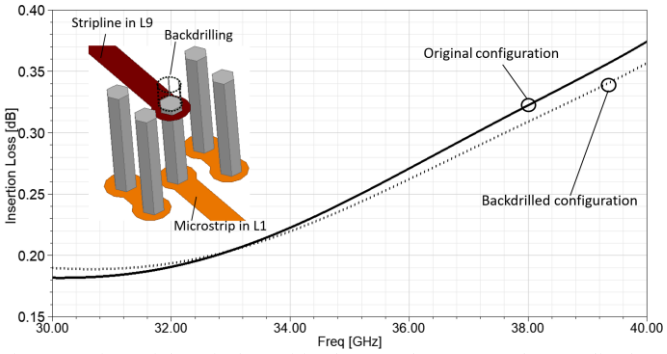


Fig. 4 Quasi-coaxial vertical transition between layers L1 and L9, realized with a central backdrilled via.

would extend beyond the stripline on L9 thus behaving as a stub. A simple and effective method to reduce the impedance mismatch caused by these stubs without changing the board buildup is to employ a back-drilling technique which removes a portion of the via from L11 to L9 with numerically controlled drill equipment. However, even in this case the via stub can be reduce but not cancelled. Indeed, in order to avoid the risk of disconnection between the via and the stripline in L9 the drilling machines has to be stopped at a safe distance of about 100um. Nevertheless, it has been evaluated that the remaining part of the stub and the dielectric discontinuity created by the drilled hole causes only an increase of 0.1 dB of the insertion losses (IL) as it can be observed on Fig. 4 which compares the IL of the original and the back-drilled configuration.

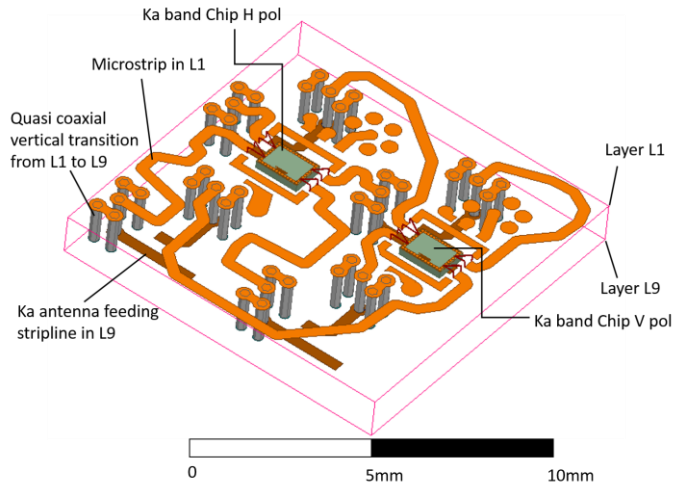


Fig. 5 Ka Band band elementary cell composed (just layers L1 and L9 are shown).

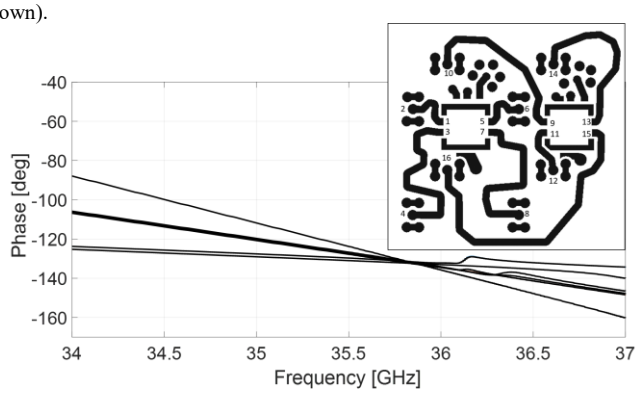


Fig. 6 Phase difference between antennas outputs and chips inputs for the 2x2 Ka band subarray . Figure shows phase of Sij where i and j indicates the port numbers. i=1,3,5,7,9,11,13,15; j=2,4,6,8,10,12,14,16.

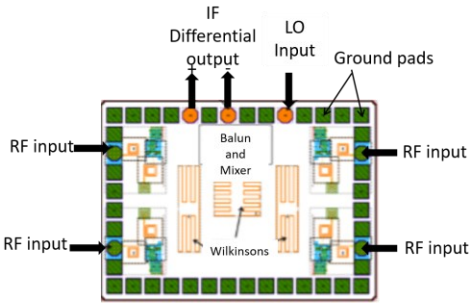
B. In-phase design of the vertical transitions and routing

All the vertical transitions used in the proposed design employ an identical architecture. Minimal differences are employed to optimize the layout of the distribution network which interconnects the elementary 2×2 sub-array of Ka-band elements with the two MMICs used for the vertical and horizontal polarizations. The involved layers, as shown in Fig. 5, are L1 and L9 incorporating the antenna input ports and the MMIC access ports, respectively. The MMIC on the left side is connected to the horizontal polarization while the vertically polarized signals are connected to the right side chip. The most critical factor in the design of this block is to ensure phase coherence of the two groups of paths driving each MMIC. The phase coherence must be guaranteed in the 100 MHz bandwidth around the central frequency (both for Ka- and X-band case) being this value determined by the Analog to Digital Converter (ADC) mounted on the ADC board (Fig. 1-b). The phase difference of the Ka-band MMIC input signals will result in lower signal to noise ratio (SNR) of the output signal. For the case at hand, the maximal phase difference dictated by the chip minimal SNR is equal to 15 degrees over the entire bandwidth [6]. In order to achieve this goal, the routes of the transmission lines interconnecting each Ka-band antenna to the corresponding MMIC have been carefully designed and optimized in the limited unit-cell area. Fig. 6 shows the phase differences between antennas outputs and chips inputs at Ka band. The maximum phase difference at the boundaries of the band (35.75GHz±50MHz) is 12 deg. A sensitivity analysis that takes into account the manufacturing tolerances of both the vertical and planar interconnections has shown that the maximum phase difference does not exceed 13 degrees.

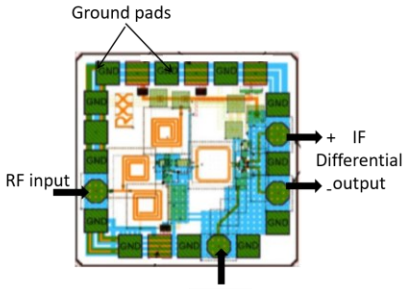
IV. CHIP INTEGRATION

As discussed in Section II, two types of MMICs are used to receive the output of the X- and Ka-band antennas. The functions of each chip are to amplify, combine and down-convert the received X- and Ka-band signals to the IF band (0-100 MHz) as requested by the ADCs. Each X-band antenna is connected to a single channel MMIC which operates the down conversion using a 9.6-GHz local oscillator (LO) signal generated off-chip and distributed across the board. The X-band chip includes a low-noise amplifier (LNA), a mixer, and an output buffer. The Ka-band MMIC is similar to the X-band one but it embeds 4 LNAs, one for each element of the sub-array. The amplified signals are then summed through a two-stage Wilkinson power combining network whose output signal is then down-converted making use of a 35.75 GHz off-chip LO. The employment of a monolithically integrated power-combining stage is essential to reduce the density of the L1 layer.

Both MMICs receive single-ended RF and LO input signals matched at 50-ohm whereas the output signal is differential and it is matched to 100-ohm in accordance to the input impedance required by the ADC used in the ADC board (see Fig. 1). A

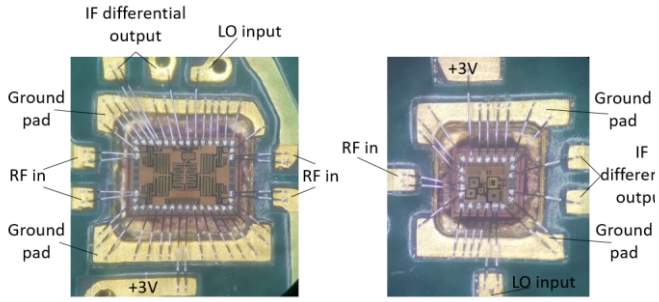


(a)



(b)

Fig. 9 Pad frame of the MMIC chip (a) Ka-Band Chip (b) X-Band Chip.



(a) (b)

Fig. 10 (a) Ka-Band Chip integrated in the top cavity; (b) X-Band Chip integrated in the top cavity.

detailed description of the chip used in this work is available in [6].

One of the most critical aspects of the RF board design is the integration of the MMICs. Bare dies are used in order to reduce the integration area. It is worth noticing that the high number of input/output ports of the Ka-band chips does not allow the use of flip chip integration techniques as the density of the traces is not compliant with a standard PCB process. For this reason, it was necessary to employ a wire bonding technique. Furthermore, in order to reduce the length of the bonds (i.e. their parasitic inductance) laser cavities were carved into the upper layers of the stack-up (from L1 to L3) to accommodate the MMICs as shown in Fig. 3. Bondwires have a diameter of 25 µm and an average length of 0.65 mm. The simulated parasitic inductance is about 500pH. Considering the limited available space around the chips on layer L1 (see Fig. 5), the bondwire inductance has been compensated inside the chip in the input matching network for each LNA. The pad frame of the

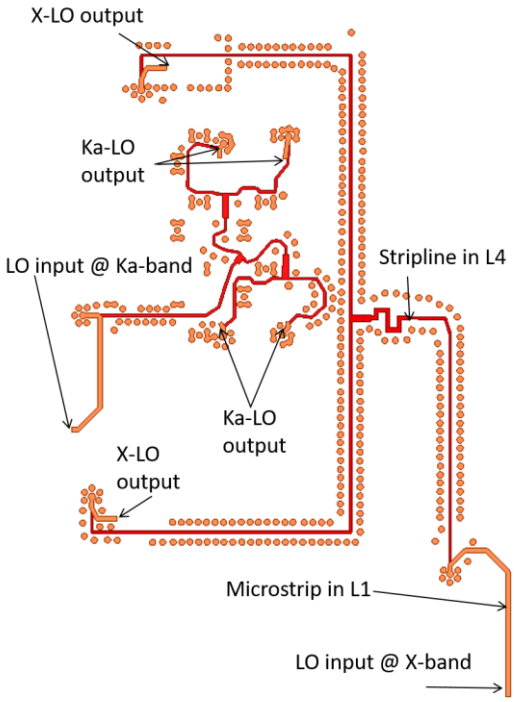
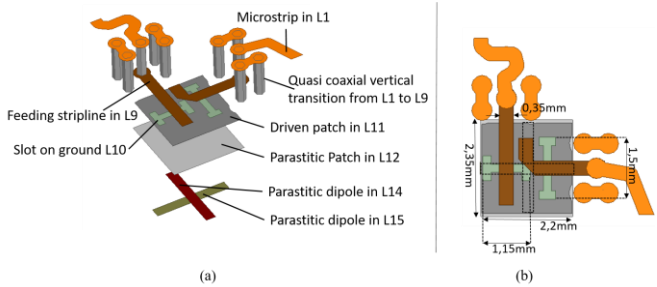


Fig. 7 Local Oscillator (LO) distribution networks at X- and Ka-band integrated in the radar tile stack-up. Just layer L1 (in orange) and layer L4 (in red) are shown.



(a) (b)

Fig. 8 Single Ka-band antenna integrated in the 15 layers stack-up: (a) 3D view (b) top view (from layer L1 to L15).

chips is shown in Fig. 7. Fig. 8 provides an image of the X- and Ka-band MMICs integrated in the manufactured radar tile prototype. Chip ground pads are wire bonded to the two microstrip pads printed near the upper and lower border of the cavity which is entirely metallized. Microstrip pads are soldered to the internal metallic walls of the cavity.

A. Local Oscillator distribution network

Two LO distribution networks are required to provide phase coherent inputs to the local oscillator ports of the Ka- and X-band chips. As shown in Fig. 2, the LO network of the single radar tile at Ka it is composed by one input and four outputs while at X band there are just two outputs. Looking at Fig. 5, it is clear that the density of the upper layer L1 does not allow the integration of these networks. For this reason, the LO networks have to be implemented in an intermediate layer (L4 in Fig. 3). Fig. 9 shows the two LO distribution networks. Two corporate feed networks have been used to guarantee phase coherence and equal amplitude at the output ports. Input and output ports are located on the upper layer L1, while the rest of the network is accommodated in the intermediate layer L4. Connection

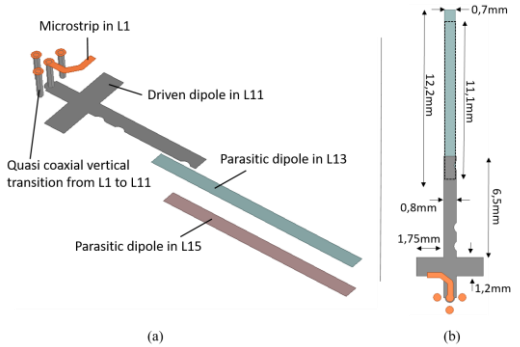


Fig. 11 Single X-band antenna integrated in the 15 layers stack-up: (a) 3D view (b) top view (from layer L1 to L15).

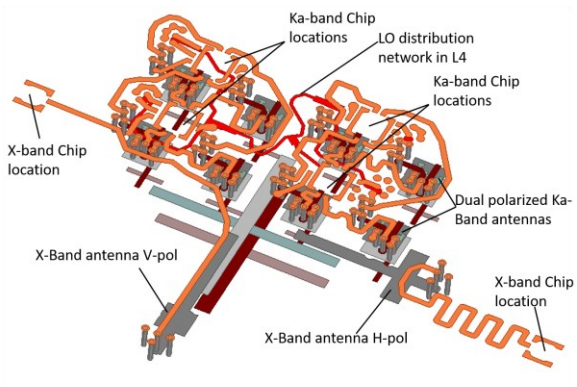


Fig. 12 Integration of the antenna arrays in the 15 layer stack-up of a signle tile. The tile accommodate two 2x2 arrays at Ka-band and two antennas at X band (see architecture shown in Fig. 2).

between the two layers is guaranteed by quasi-coaxial vertical transitions similar to the one presented in section III.A. As shown in Fig. 9 several shielding vias have been placed around the stripline to avoid the excitation of unwanted modes in the parallel plate between L3 and L5 ground layers.

B. *Power Distribution Network*

A power distribution network has been integrated in the internal layer L6 of the radar tile to distribute low noise and stable power to the MMICs. The maximum absorbed current by the Ka- and X-band chips is equal to 40 mA and 20 mA, respectively. Therefore, the 10 MMICs present on each tile absorb 660 mW of DC power.

V. ANTENNAS INTEGRATION

The basic principles underlying the Ka- and X-band antenna design have been presented in [6] where they have been validated using a simplified 7-layer mock-up. In the present work, the antennas have been optimized to fit into the 15-layer stack-up shown in Fig. 3.

A. *Ka-band antenna integration*

Ka-band antennas are dual-polarized stacked patches electromagnetically coupled to the feeding lines through slots (**Errore. L'origine riferimento non è stata trovata.**). The driven patch has been integrated in the layer L11 of the stack-up. A slot in the ground layer L10 is used to couple the patch with the feeding stripline printed in L9. Connection between microstrips in the top L1 layer and feeding strips in L9 is

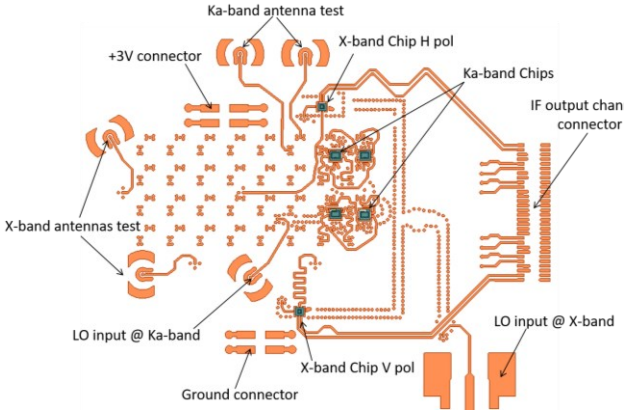


Fig. 13 Final configuration of the board (just layer L1 is shown).

obtained using the quasi-coaxial vertical transitions described in Section III.A. Two orthogonal parasitic dipoles and a patch have been added in layers L12, L14 and L15 to improve the radiation patterns and gains.

B. *X-band antenna integration*

The X-band antenna is realized with a pair of cross-dipole antennas printed on layers L13 and L15 (Fig. 11) proximately coupled to a driven dipole printed on L11 . In order to reduce the number of layers in the proposed stack-up, the Ka-band driven patch and the X-band feed are arranged on the same layer (L11). A quasi-coaxial vertical transition is used to connect the antenna to the microstrips in L1. As for the Ka-band case, parasitic elements are used to enhance the gain and the bandwidth of the antenna. As shown in Fig. 3, 2mm of foam are used as spacer between the dipole in L13 and the dipole in L15. Small cuts have been added on the driven dipole to maintain an appropriate distance between the dipole and vias placed near the antenna.

C. *Antenna array integration*

A partial view of the tile layout is shown on Fig. 12 where are shown 2 X-band antennas and 8 Ka-band elements. In the same figure is also visible (in red) the Ka-band LO distribution network integrated in the intermediate layer L4 (see Section IV.A). In order to validate the manufacturing process of the tile, the remaining Ka-band antenna elements were not bonded to the MMICs but were fed by 4 connectors SMD connectors (Fig. 13) to allow a direct measurement of the antenna parameters. Furthermore, the signal detected at the output of these antennas was also used as a reference during the chip measurements (see Section **Errore. L'origine riferimento non è stata trovata.**-B).

VI. STACK-UP MANUFACTURING PROCESS

The radar tile prototype has been fabricated using the 15-layer stack-up presented in Fig. 3. A complex manufacturing procedure with tailored solutions was used during the production steps. In standard PCB manufacturing process layers of copper foil, prepreg and core materials are sandwiched together under high temperature and pressure to produce multilayer assemblies. In this work, an innovative process that uses a dedicated fusion bonding technique has been employed. In this process, developed by Nuova Eurotar s.r.l, Italy, different core layers are glued together without using any

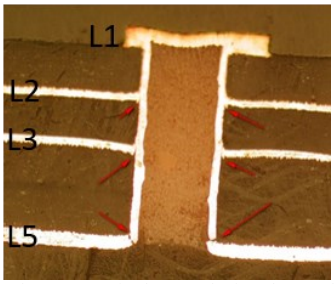


Fig. 14 X-ray image of a type#2 via damaged after the production step#3

prepreg. In this way, the layup is more homogeneous in the vertical direction thus limiting the uncertainties typically associated to such a complex manufacturing process. Furthermore, this technique reduces the roughness of the printed striplines thus limiting the transmission losses. Indeed, in a standard manufacturing process a copper roughening step is needed to enhance the bond between the oxidized copper and the prepreg layers.

The fabrication process of the advanced multilayer PCB can be divided in six main steps as follows (Fig. 15):

- Step#1: Manufacturing of the sub-board composed by layers from L1 to L5 (Type#2 vias are fabricated in this step);
- Step#2: Manufacturing of the sub-board composed by layers from L6 to L11;
- Step#3: The two sub-boards are bonded together under high temperature and pressure to produce an 11-layers assemblies.
- Step#4: type#1 vias are fabricated, and backdrilling is performed where necessary;
- Step#5: layers from L12 to L15 are added.
- Step#6: laser drilling and metallization of the cavities used to accommodate MMICs are performed.

Step number 3 is the most critical one, because high pressure and temperature used to bond together the two boards, can damage the vias fabricated in step#1; this might be caused by the deformation of the laminate used between L1 and L5. Fig. 14 shows an x-ray image of a via damaged after the competition of step#3. Arrows show some breaking point where the via has lost the electrical connection with inner ground layers L2, L3 and L5. This problem was solved reinforcing the vias fabricated in step#1 by the following measures:

- After the metallization, the inner part of the vias were filled with a special reinforcing;
- Maximum diameter of the vias was reduced to 0.2mm;
- Circular pads were added at the top (layer L1) and bottom (layer L5) of each via.
- Rogers 2929 (instead of Ro5870) was used between layers 5 and 6: this dielectric allows using a lower pressure/temperature to bond together the two boards in step#3;

Fig. 16 shows the top and bottom view of the successfully manufactured board.

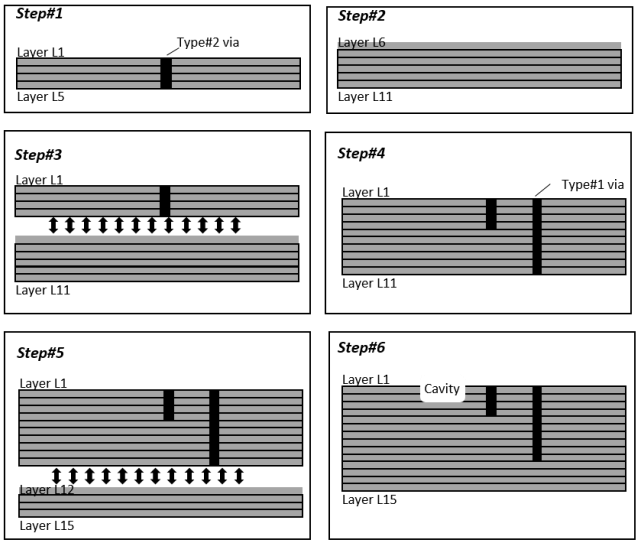
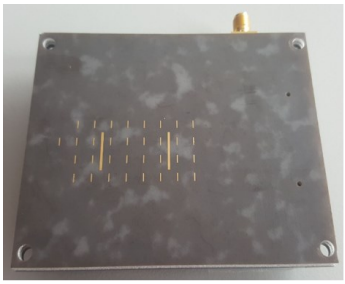
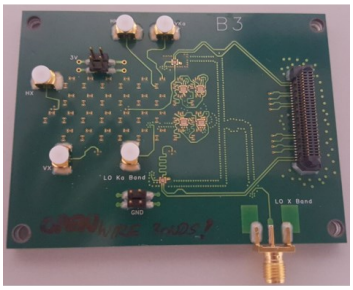


Fig. 15 PCB stack-up manufacturing steps


(a)



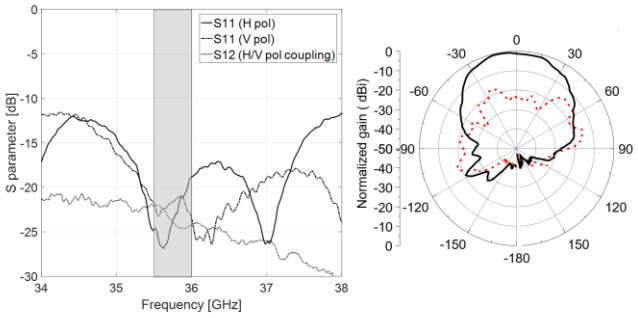
(b)

Fig. 16 Photograph of the manufactured board: (a) view form layer L15; (b) view from layer L1.

VII. Experimental Validation

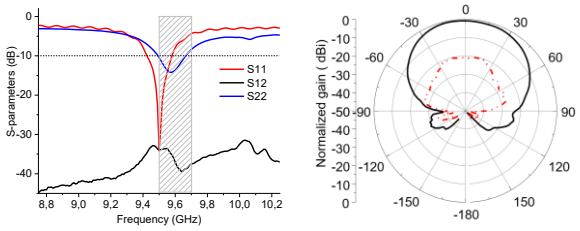
The objective of the experimental validation of the board was twofold. First, it was necessary to assess the manufacturing process. Second, measurements on the entire receiving chain were operated to verify the coherence of the experimental data with the design employing, for the first time, a fully integrated sub-system. For this reason, two types of tests were planned within the same tile:

- A sub-set of the tile radiating elements was fed using SMD connectors to directly characterize the S-parameters and the radiation patterns;
- The entire down-conversion chain including both antennas and MMICs (using the configuration shown in Fig. 12) was validated illuminating the board with



(a) (b)

Fig. 17(a) Measured S parameters of the Ka-band antenna; (b) Co-polar and cross-polar normalized radiation pattern of the vertically polarized Ka-band antenna at 35.75 GHz. Continuous line: co-pol, dashed line: cross-pol.



(a) (b)

Fig. 18 (a) Measured S parameters of the X-band antennas; (b) Normalized co-polar and cross-polar radiation pattern of the X-band horizontally polarized antenna at 9.5GHz. Continuous line: co-pol, dashed line: cross-pol.

horn antennas and measuring the IF signals of the six output channels.

In the following, two sets of measurements will be presented.

A. Direct antenna measurement

As outlined in the previous section, antennas integrated in the tile are not directly accessible because they are connected to the chips. For this reason, in order to characterize the antenna performances within the final stack-up, one Ka- and two X-band antennas were employed as test vehicles and fed with SMD connectors. In particular, the Ka-band radiator was fed with two ports for the V and H polarization placed on layer L1 while the V and H polarized elements in the X-band were individually fed. Fig. 16 shows the assembled prototype board that was used for the measurements. Fig. 16 (a) shows the antenna layer (L15 in Fig. 3) and (b) the layer with chips and connectors (L1 in Fig. 3).

Fig. 17 (a) shows the measured S-parameters of the Ka-band antenna. Matching for both antenna ports (H pol and V pol) are shown. Coupling between the two polarization ports is lower than -23dB over the whole bandwidth. Fig. 17 (b) shows the normalized gain of the Ka-band antenna when only the horizontal polarization port is excited. A similar pattern is obtained in case of vertical port excitation. The measured peak gain is 6.8 dBi at 35.75 GHz.

(a) (b)

Fig. 18 (a) shows the measured S-parameters of the X-band antenna. Matching for both antennas (H pol and V pol) are shown. Coupling between the two polarizations is lower than -33dB over the whole bandwidth. The reflection coefficient of the two polarizations is roughly acceptable as it is narrower than expected bandwidth. This problem was caused by a minor manufacturing error. Indeed, a 1mm foam layer between L13 and L14 (see Fig. 3) was used in instead of 2mm. Measurement tests and simulations confirmed that this manufacturing error has a minor effect on the performance of the tile. In particular, the main effect is confined to the X band antennas matching. For this reason, and in view of the high cost/time of manufacturing, it was decided that a new prototype was not necessary.

(a) (b)

Fig. 18 (b) shows the normalized gain of the X-band horizontally polarized antenna at 9.5GHz. A similar pattern is obtained for the vertically polarized radiator. The measured peak gain is 11.7 dBi.

B. Antenna & chip measurement procedure

Results presented in the previous section demonstrate the correct behavior of the radiators integrated in the full PCB board. In this section, the whole receiving chain composed by antennas, chips and all other integrated components was tested. Fig. 19 and Fig. 24 show the measurement setup used to characterize the tile board. For each band, the tile has been excited by signals radiated by X- and Ka-band horn antennas placed in the far field area.

As a first step, signal levels received by the X- and Ka-band antenna test elements were measured. This measurement is necessary to evaluate the signal power present at the input of X- and Ka-band MMICs. In a second phase, the output IF signals of the X- and Ka-band chips is measured. These two steps, along with de-embedding techniques, are necessary to identify the conversion gains of the MMICs. Moreover, the P1dB point and DC current consumption was also measured. Conversion gain has been measured versus LO frequency (by keeping constant the RF frequency), LO power, RF power, supply voltage and RF frequency (being the LO frequency kept constant).

X-band measurements were done with 50 cm distance between the horn antenna and the board, while at Ka-band the illuminating horns were positioned 25 cm apart. The goal of the measurement is to verify that the X- and Ka-band receiver chips have similar performance on the prototype board as for the on-wafer chip measurements presented in [6].

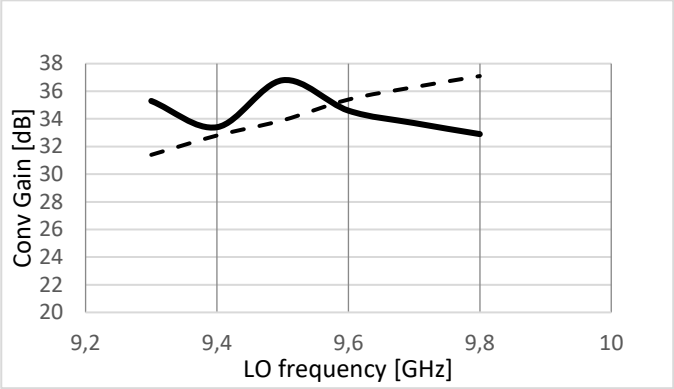


Fig. 20 Measured conversion gain of the X-band receiver vs. LO frequency. Continuous line: current prototype; dashed line: on wafer measurement.

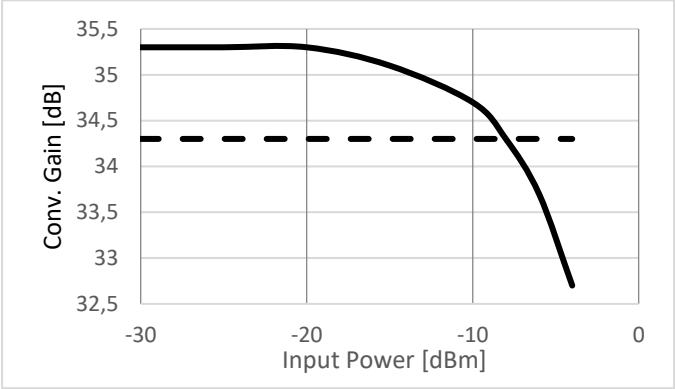


Fig. 22 Measured conversion gain of the X-band receiver vs. RF input powe Continuous line: current prototype; dashed line: on wafer measurement.

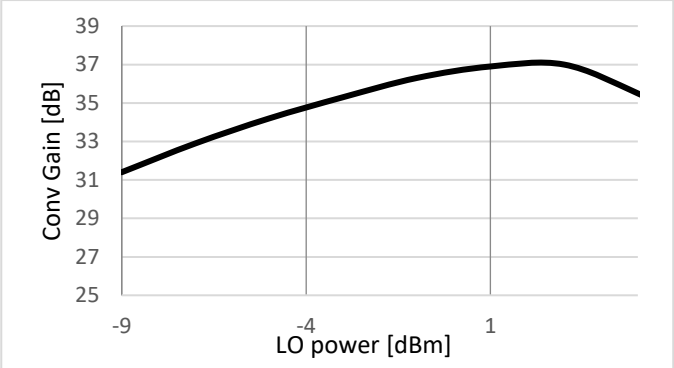


Fig. 21 Measured conversion gain of the X-band receiver vs. LO power.

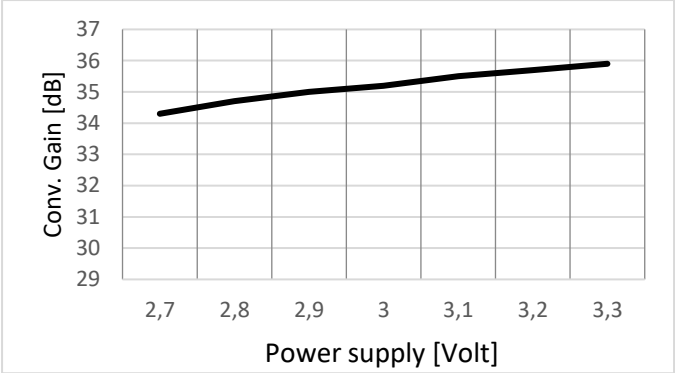


Fig. 23 Measured conversion gain of the X-band receiver vs. supply voltage.

C. *Measurement results for the X-Band Receiver*

X-band measurements have been performed using the following equipment (Fig. 19):

- RF signal source: Agilent E8267D signal generator (up to 20GHz);
- LO signal source: R&S SMF 40 signal generator (up to 43.5 GHz);
- IF output/antenna output - measured single-ended with Rohde & Schwarz Signal Analyzer FSV 30 GHz;
- 8 channel voltage source;
- X-band horn antenna (with coax input);

Fig. 20 shows comparison of the measured conversion gain vs. LO frequency for constant IF frequency of 100 MHz. Supply voltage for all measurements is 3V while the expected current consumption for 2 X- and 4 Ka-band MMICs is equal to 182 mA (2*25+4*33=182mA). Conversion gain at 9.6 GHz is 34.6 dBm while 35.4 dBm were measured on-wafer **Errore. L'origine riferimento non è stata trovata.**. Fig. 21 shows the conversion gain versus the LO power from the generator. All the measurements were performed with an LO power of -3 dBm where the gain is 2 dB lower than the maximum gain. Power level at the board connector is -5.2 dBm. Fig. 22 shows conversion gain versus RF signal generator power. P1dB at the output is -2.1 dBm single-ended or 0.9 dBm differential. Fig. 23 shows the conversion gain versus supply voltage. As it can be observed, a gain variation of less than 1 dB is shown when the voltage is varied by 10%.

D. *Measurement Results for the Ka-Band Receiver*

Ka-band measurements have been performed using the following equipment (Fig. 24):

- RF signal source: R&S signal generator SMR100A (up to 43.5 GHz);
- LO signal source: R&S signal generator SMR60 (up to 60 GHz);
- IF output/antenna output - measured single-endedly with Agilent E4448A Spectrum Analyzer 50 GHz;
- 8 channel voltage source;
- Ka-band horn antenna with waveguide input + coax to waveguide adapter;

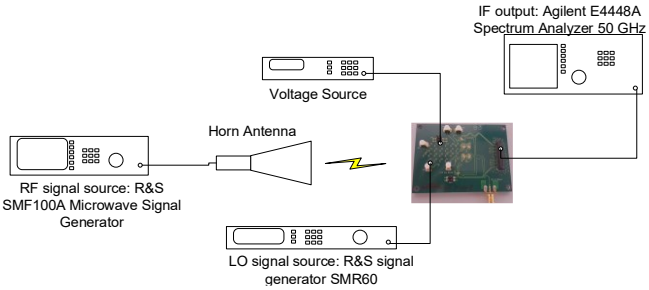


Fig. 24 Measurement setup at Ka-band

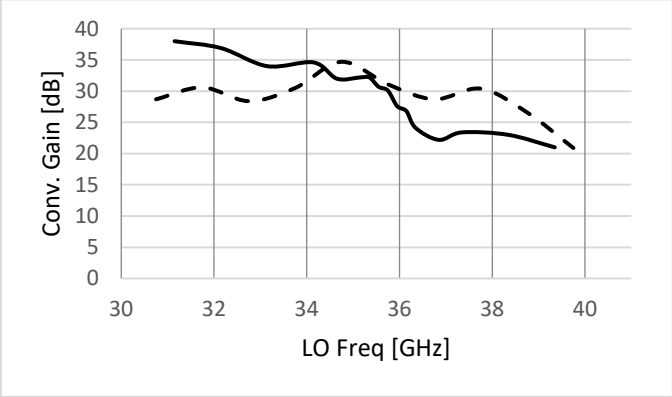


Fig. 25 Measured conversion gain of the Ka-band receiver vs. LO frequency. Continuous line: current prototype; dashed line: on wafer measurement.

Fig. 25 shows comparison of the measured conversion gain vs. LO frequency of the Ka-band receiver chips for constant IF frequency of 100 MHz. The bias voltage in all measurements is 3 V. Measured conversion gain at 35.75 GHz is 30.1 dB while 30.7 dB were measured on the on-wafer configuration [6].

Fig. 26 shows the conversion gain versus LO power. All the measurements were done with an LO power of 3 dBm, i.e. approximately 2 dB below the maximum gain. The power level measured at the board connector is -1.8 dBm. Fig. 27 shows the conversion gain versus RF signal generator power. P1dB at the output is -3.6 dBm single-ended or -0.6 dBm differential. As for the X-band case, the conversion gain is highly stable with respect to the supply voltage variations (see Fig. 28).

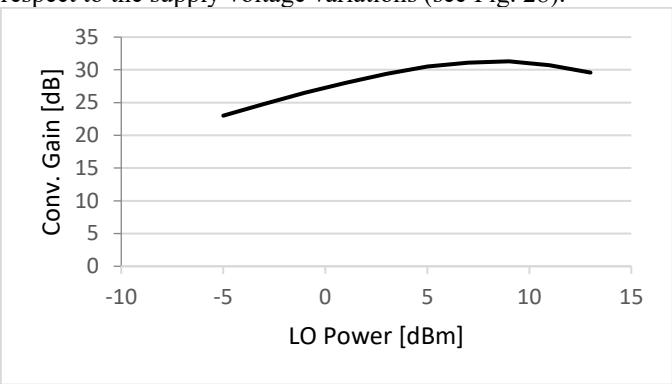


Fig. 26 Measured conversion gain of the Ka-band receiver vs. LO power.

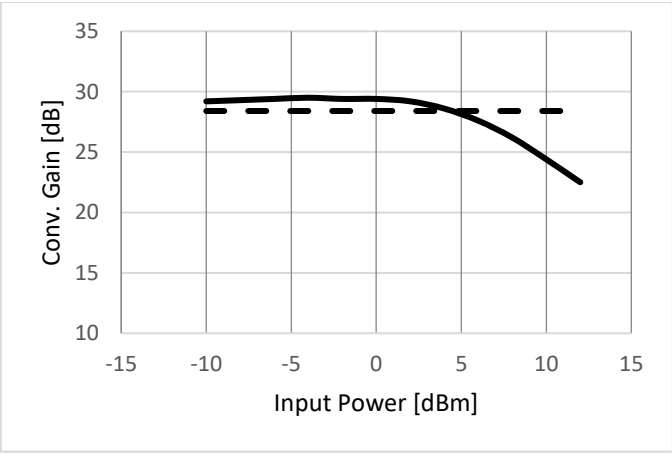


Fig. 27 Measured conversion gain of the Ka-band receiver vs. RF input power. Continuous line: current prototype; dashed line: on wafer measurement.

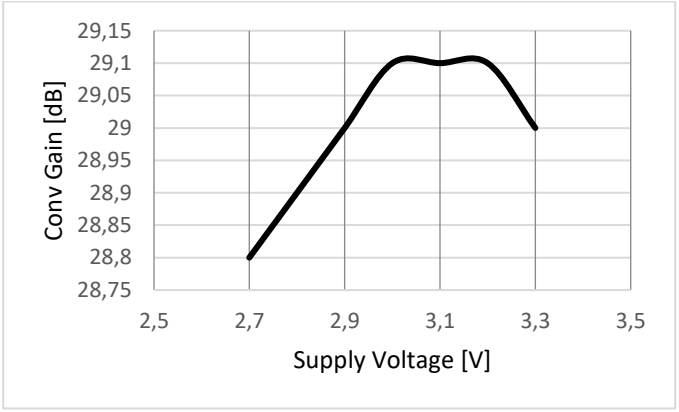


Fig. 28 Measured conversion gain of the Ka-band receiver vs. supply voltage.

E. Final remarks

The experimental assessment of the integrated tile has shown that the X- and Ka-band receiving chains behave as expected with a chip conversion chain substantially agreeing with the on-wafer measurements [6]. Limited differences are present and they appear to be within the expected chip-to-chip variations. Measured S-parameters were extrapolated through a de-embedding procedure using the antenna ports as a reference. The agreement between measured and simulated values confirms the validity of the proposed integration process and of the associated design. It was not possible to measure the noise figure of the whole Ka-band MMICs but the data of the single LNA were evaluated in [6]. However, the on-chip power combining was characterized indirectly through the estimation of the conversion gain of the MMIC which was in agreement with the single channel value plus 12 dB.

VIII. Conclusion

In this paper, a first example of highly integrated dual-band dual-polarized Synthetic Aperture Radar RF module was presented. The proposed radar tile integrates all the RF components, i.e. antennas and down-conversion stages, required to compose the RF front-end of a DBF SAR instrument. The architectural approach is fully modular and it allows the scalability of the design as dictated by the mission specifications.

Although conceived for experimental purposes, the proposed demonstrator is conceived for a standard production process as it employs standard High Density Interconnect (HDI) technology. Custom solutions have been devised and tested to adapt the HDI process to the complex stack-up necessary to implement the proposed tile. The main challenge was to design a low-cost SAR tile at the highest limit of complexity for the proposed technology. Experimental results demonstrate the validity of the overall approach. Indeed, the results of the integrated tile are well matched with the behavior of the single blocks individually tested in [6]. A conversion gain of about 35 and 30 dB was demonstrated in the X- and Ka-band, respectively. Thanks to its compactness, the proposed RF board tile can be considered an example of a key building block enabling a new range of EO applications based on small satellite platforms.

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