

0.25- μm BiCMOS System-on-Chip for K-/Ka-Band Satellite Communication Transmit–Receive Active Phased Arrays

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Abstract—The first millimeter-wave system-on-chip for dual-band phased array applications is presented as a proof of concept for K-/Ka-band (20/30 GHz) satellite communication on-the-move applications. Each chip includes four transmit (Tx) and two receive (Rx) channels working at Ka- and K-band, respectively. The proposed architecture enables a half-duplex operating mode in two different bands. Its development was driven taking into account the integration into a realistic Tx/Rx shared aperture phased array architecture. Full amplitude and phase control are provided for each channel with high granularity (65536 states). The measured results demonstrate the validity of the proposed chip architecture, even though the channel output power and the noise figure (NF) are not in full agreement with the simulations. In Tx mode, the channel provides 9.47 dB of gain with 4.19-dBm output power at 1-dB compression. In Rx mode, the channel gain is 21.6 dB with an NF of 5 dB. In a scenario with 5.265° phase steps and 8-dB amplitude tapering capability, the amplitude and phase root-mean-square (RMS) errors within the Tx bandwidth (29.5–30.8 GHz) are equal to 0.52 dB and 3.74°, respectively. The amplitude and phase RMS errors in the Rx bandwidth (19.7–21 GHz) are equal to 2.05 dB and 12.11°, respectively. The chip consumes 340 mW in Tx and 242 mW in Rx mode and occupies 3.3 × 3.5 mm².

Index Terms—K-band, Ka-band, monolithic microwave integrated circuit (MMIC), phase shifter, phased array, SatCom on the move (SOTM), system-on-chip (SoC), vector modulator.

I. INTRODUCTION

SATELLITE communication (SatCom) systems, operating at K-/Ka-band, have been identified as pillars of the “future internet” architecture, which is expected to merge

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the patchwork of mobile and fixed networks into a single communication infrastructure. Therefore, it will be essential to develop user terminals for satellite communications on the move (SOTM), which can be easily integrated on land, maritime, or airborne vehicles. They should provide coverage over a wide scanning range, high angular scanning resolution, and simultaneous up- and downlink operation. Phased arrays are the most viable solution to meet such requirements. However, in this context, their architecture becomes particularly complex, posing significant challenges in terms of integration. They require a transmit (Tx)/receive (Rx) module per array element to provide amplitude and phase control along with an amplifying stage. Although in the past several solutions at similar frequencies were designed employing GaAs [1]–[4] or InP [5], [6] building blocks, these semiconductor technologies cannot be used for applications requiring higher integration. In fact, SiGe BiCMOS is a competitive technology here due to its ability for high integration density. For example, in [7], a 30–38 GHz 4-b phase shifter integrated with a low-noise amplifier (LNA) in a 0.12- μm SiGe BiCMOS process was proposed. A similar configuration, combined with a variable-gain amplifier (VGA) was also demonstrated for single-ended and differential Ka-band phased array modules [8]. A Tx/Rx module operating in Ka-band was proposed in [9] combining on the same chip a power amplifier (PA), an LNA, a single 4-b phase shifter cascaded with VGA, and a pair of single-pole-double-throw (SPDT) switches.

Having multiple Tx and Rx units monolithically integrated on a single chip will be a crucial feature in SOTM phased arrays where thousands of array elements are expected to be integrated into the same radiating aperture. The array lattice and, in turn, the size of the unit cell cannot be much greater than $\lambda/2$, at the highest frequency, to avoid the formation of grating lobes. As a result, the integration of chips, control signals, and distribution network routing is extremely challenging, even using high-resolution multilayer printed circuit board (PCB) technology [10], [11]. To cope with this issue, the most viable solution is to develop chips with a higher number of Rx/Tx channels, where part of the distribution network is monolithically integrated with the RF and mixed-signal blocks.

Several multicore configurations have been proposed [8], [12]–[14], which combine, on the same chip, up

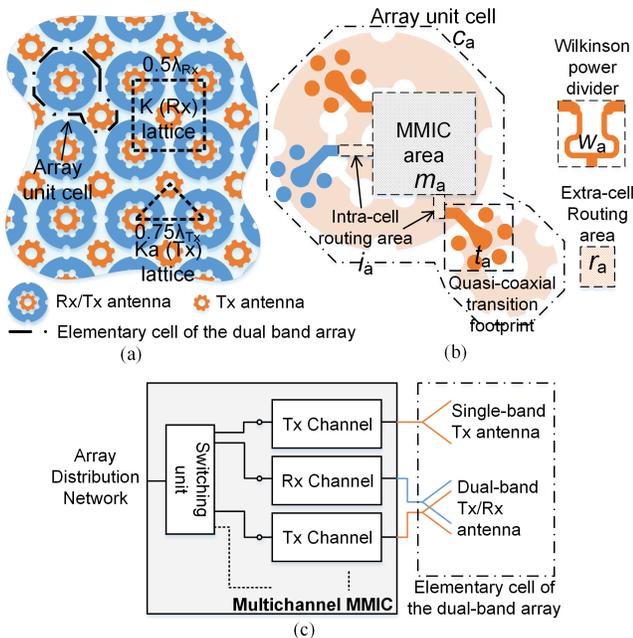


Fig. 1. (a) Dual-band single aperture phased array configuration. (b) Area budget of the array elementary cell for the case of an integrated circuit serving three array elements. (c) Multichannel chip architecture for the dual-band (Tx/Rx) SOTM phase array.

to eight channels, all operating at the same frequency, namely, in the Ka-band. One of these ICs was developed within the framework of the European FLEXWIN project, where a SiGe BiCMOS Ka-band monolithic microwave integrated circuit (MMIC) was developed for a single-band beam steering reflectarray antenna [15], [16]. This architecture combines four Rx/Tx modules, a mixed-signal control unit (MSCU), SPDTs based on the RF-MEMS, and high-voltage generation in the same device. Reporting on work within the same European project, this paper expands upon a similar concept by introducing the first multichannel chip having Rx and Tx channels in two different bands. In fact, the chip presented in this paper is the first example of an MMIC designed in compliance with SatCom frequency allocations requiring the Rx at K-band (19.7–21 GHz) and the Tx channel in the Ka-band (29.5–30.8 GHz). As will be shown, the ability to embed into the same chip multiple cores operating at two different bands is essential for developing SOTM single aperture user terminals or for any other dual-band shared aperture phased array design where the frequency separation between the Tx and Rx channels cannot be covered with wideband components.

The proposed hexa-channel MMIC was developed taking as a reference case the new compact dual-band phased array lattice introduced in [10] and reproduced in Fig. 1 for the sake of clarity. In this configuration, the proposed chip greatly reduces the integration complexity at the system level for two main reasons. First, a single MMIC is designed to drive six channels by embedding a relevant part of the phased array distribution network on-chip which would be otherwise impossible to locate on the PCB carrier given the limited

available area. Second, each chip integrates an MSCU used to configure the MMIC through a serial two-wire bus, thus significantly reducing the necessary interface signals.

II. MULTICHANNEL INTEGRATED CIRCUIT ARCHITECTURE

A. Application Context

Although not yet available to the market, arrays with the 2-D electronic scanning capability are receiving an increasing attention for their application to SOTM systems. They are expected to provide an unquestionable advantage in terms of compactness and cost when compared to antennas with mechanical steering. However, to date, all the academic and industrial research activities on this topic have been focused on the use of two distinct arrays for the downlink (Rx) and the uplink (Tx) links. Yet, this configuration almost doubles the area occupied by the SOTM user terminal, thus increasing the installation complexity, especially for aeronautical applications. As an alternative to this approach, this paper is based on an antenna configuration that can integrate into a single aperture dual-band phased array capable of operating in both uplink and downlink.

The implementation of such an SOTM system requires the development of a particular array lattice, shown in Fig. 1(a), where the dual-band (Tx/Rx) radiating elements are interleaved with single-band elements (Tx). Both radiators are placed on the top of the same PCB board using a square and a triangular lattice, respectively. The two lattices partially overlap in a way that the interelement spacing is equal to $0.5\lambda_{Rx}$ and $0.75\lambda_{Tx}$ for the Rx and Tx array, respectively. As demonstrated in [10], this particular configuration avoids grating lobes within the $\pm 60^\circ$ scanning range in both bands. The elementary cell of this dual-band array arrangement is composed of a combination of a Tx/Rx antenna and a Tx antenna, and it occupies a PCB area c_a of 52 mm^2 as shown in Fig. 1(b).

The limited cell size makes the chip integration and the routing of the distribution network extremely challenging. To simplify the array architecture, a single distribution network is used for both K- and Ka-bands. Therefore, each chip should contain a power combining/dividing stage and a switching unit to provide a single input–output connection to the distribution network. Furthermore, as shown in Fig. 1(b), each antenna element is self-duplexing providing single Tx and Rx ports with an isolation higher than 30 dB [10]. The feeding port of each radiating element is connected through a quasi-coaxial vertical transition to the bottom layer of the PCB stackup where the chips are integrated. In the stackup described in [10] and [11], each transition occupies an area (t_a) of $1.7 \times 1.9 \text{ mm}$.

Based on this data, the optimal configuration of the chip is defined by quantitatively evaluating the impact of the number of channels embedded into a single MMIC in terms of PCB density on the array back-end layer. In the simplest case, each chip should serve a single array unit cell. Therefore, the three RF channels, a power dividing stage, a switching block and the digital controls have to be monolithically integrated on the

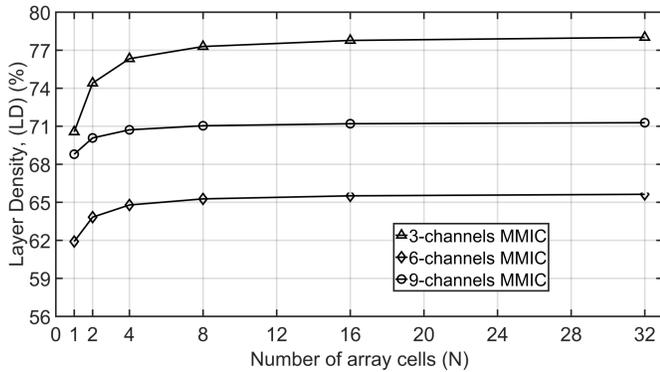


Fig. 2. LD for three multichannel integrated circuit configurations.

same MMIC served by one MSCU. Therefore, the portion of unit cell area consumed for the MMIC integration in one PCB layer is $b_a = 3t_a + i_a + m_a$ where i_a is the area required for intracell routing which is estimated to be equal to 2 mm^2 , and m_a is the size occupied by the chip including the bonding area.

The design of an array with an even number of array unit cells N would require $N-1$ Wilkinson power dividers to connect the different chips and N routing lines, each of which would occupy, for the stackup at hand [10], [11], an area of $w_a = 2 \times 2 \text{ mm}^2$ and $r_a = 4 \times 4 \text{ mm}^2$, respectively. It is worth noting that, in principle, the area occupied by the routing circuits, i_a , and r_a , can be reduced by using additional stripline layers in [10]. However, although this solution would simplify the distribution network topology, it would not result in any significant reduction of routing area on the back-end layer due to the need to use multiple quasi-coaxial transitions between the microstrip layer and stripline layers.

For the configuration at hand, the layer density (LD) can be related to the number of array unit cells using the following expression:

$$\text{LD}(N) = \frac{N \cdot (b_a + r_a) + (N - 1) \cdot w_a}{N \cdot \gamma \cdot c_a} \quad (1)$$

where γ is the number of array unit cells that can be controlled by a single MMIC. For the tri-channel chip, γ is equal to 1, whereas γ equal to 2 and 3 corresponds to MMICs embedding six and nine RF channels, respectively. Based on the results to be presented in Section IV, it can be assumed that for γ equal to 1, 2, and 3, m_a equals $3 \times 3 \text{ mm}^2$, $5 \times 5 \text{ mm}^2$, and $7.5 \times 7.5 \text{ mm}^2$, respectively. Fig. 2 shows that, as the number of array elements increases, the LD saturates. It is evident that even when integrating three RF channels on the same chip, it is not possible to implement the dual-band phased array because the PCB density in the back-end layer would tend to 80%, thus not leaving enough space to route the distribution network to feed the N array unit cells. On the other hand, using MMICs with six or nine channels reduces the PCB density to 65% and 72%, respectively. It is worth noting that this tendency in favor of the hexa-channel configuration ($\gamma = 2$) persists even when the area occupied by the nine-channel MMIC is reduced down to $6.9 \times 6.9 \text{ mm}^2$.

B. MMIC Architecture

The technology used for the development of the chip presented in this paper, a 0.25- μm SiGe:C BiCMOS process with f_T/f_{max} of 120/140 GHz, was provided by IHP GmbH. It offers five metal layers allowing the combination, in a single monolithic solution, of high-frequency heterojunction bipolar transistors (HBTs), CMOS digital, and mixed-signal blocks.

To the authors' knowledge, no design has been ever undertaken which can be adapted to the dual-band phased array configuration of Fig. 1 or, in general, to any configuration where the frequency separation between the transmitting and receiving channels is comparable to the case at hand. For example, the multichannel Ka-band chip reported in [14] and [18] employs dedicated amplification stages for each Tx or Rx channels but the phase shifter unit is shared between two channels through a switch network. Unfortunately, this solution can only be used if the transmitting and receiving frequencies are located within the bandwidth of all the devices shared by the two paths (i.e., the phase shifter and the switching network).

To solve this issue, an alternative architecture is introduced in Fig. 3, which can be employed for K/Ka SatCom systems and for any other application having Tx and Rx channels in two different bands. The proposed MMIC includes two Rx and four Tx channels fully reconfigurable in amplitude and phase through dedicated vector modulators, namely, VM_{Rx} and VM_{Tx} , respectively. The Rx amplification stage consists of an LNA cascaded with an additional LNA used as a gain block (GB). In the Tx channels, a PA is used with an intermediate gain block capable of driving the PA up to its compression point. The six RF channels of the integrated circuit are divided into two symmetrical halves connected to the distribution network port through a wideband Wilkinson power divider/combiner (WPC), reported in [17]. The chip can operate in Rx and Tx modes, depending on the configuration of the switch networks connected to each branch of the WPC. In Tx mode, the signal received from the distribution network is equally split and delivered to the four Tx channels through the switch networks, which also ensure isolation between them. In Rx mode, the channels' output signals are combined into the distribution network. The blocks in the unused path are powered down.

The MMIC RF blocks are controlled by the MSCU. The controlling data is received from the phased array digital bus through an inter-integrated circuit (I^2C) slave unit. The address of each chip is set by six intrachip pads, which can be tied to 0 or 2.5 V. This solution, chosen for maximum flexibility during the development phase, can be applied also to large-scale arrays, which would likely be divided into tiles, where each of them represents its own address space. The primary function of the MSCU is to generate six pairs of voltage signals that are used to set the amplitude and phase responses of the vector modulators embedded on-chip.

C. Link Budget and MMIC Requirements

The main MMIC requirements, expressed in terms of Tx channel output power and Rx channel noise figures (NFs), were based on the link budget analysis for SOTM aeronautical

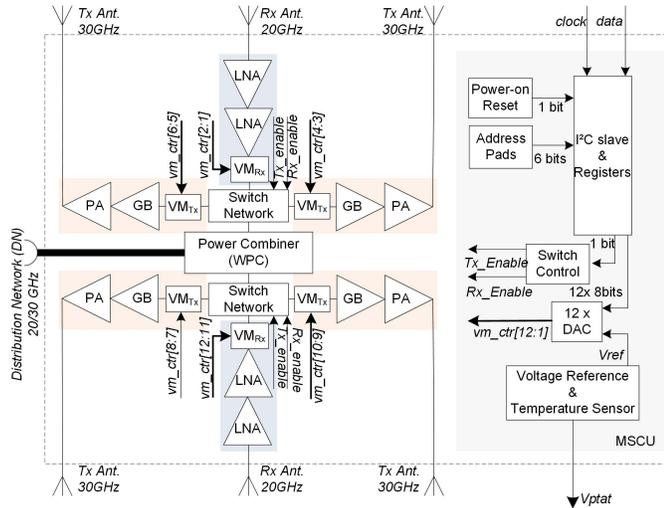


Fig. 3. Functional block diagram of the developed integrated circuit.

terminals which require beam steering of $\pm 60^\circ$ both in azimuth and elevation.

For the Tx path, the typical G/T coverage of the satellite antenna on the ground is 16 dB/K, and it requires the Tx signal transmitted by the user terminal to reach the satellite antenna with an S/N of 10 dB. Hence, this is achieved if the SOTM user terminal has an EIRP higher than 53 dBW within its main beam [19]. The fulfillment of this requirement depends on the maximum power which can be generated by each Tx channel, the gain of each array cell, the interconnection losses and the number of array elements. For the SiGe BiCMOS technology available in this research project, the power generated by each Tx channel can be expected to be equal to 13 mW. Taking into account that the antenna gain is 4.4 dBi [10], the power back off due to the linear modulation is equal to 6 dB, and the interconnection losses are equal to 1.4 dB [11], it can be calculated that, in the case of uniform amplitude, the number of array elements necessary to obtain the required EIRP is equal to about 5600.

A similar analysis can be performed for the downlink taking into account that Ka-band satellites make use of spot beams where the satellite EIRP is higher than 56 dBW [20]. To achieve an S/N higher than 10 dB at the user terminal [21] the receiving antenna G/T should be greater than 10 dB/K. The actual value of G/T depends on several parameters, the most important ones being the level of noise inherent in the receiving system, the interconnection losses and the noise temperature of the sky, which varies with the elevation angle. Assuming a receiving antenna noise temperature of 60 K [22] and an overall antenna efficiency of 50% [10], the required number of elements in the Rx array is equal to approximately 4000 when the NF of each Rx channel is equal to 5 dB. A variation in the NF results in a different number of elements in the Rx array. For example, for $NF = 4$ dB, the Rx array size decreases to 3000 elements, while for $NF = 6$ dB, it is 5000.

It is worth noting that the design architecture shown in Section II-B is driven by the integration requirements and by the

antenna array lattice [10]. Nevertheless, the idea of having four Tx and two Rx channels for each chip is also coherent with the SOTM user terminal configuration. Indeed, by applying an 8-dB amplitude tapering in the array, as required to lower side lobes and to match the radiation masks [19], the number of Tx elements would be about double the Rx ones. Thereby, this design considers a 64×64 (4096) Rx elements array and the 4:2 channel ratio leads to 90×90 Tx elements.

III. MIXED-SIGNAL CONTROL UNIT

The proposed MMIC transceiver requires 13 control registers, which are configured through an I²C slave module provided by IHP GmbH. Thus, the controlling signals are reduced to two connections, i.e., data and clock. This bus provides 400-kb/s throughput with a dynamic power consumption in the microampere range from a 2.5-V supply. The I²C slave and its registers occupy an area of $356 \times 257 \mu\text{m}^2$, while the address pads require $605 \times 250 \mu\text{m}^2$.

The MMIC is reset to a known initial state at power-up or after a brownout event by the power-on reset circuit reported in [23]. This block provides a precise bandgap-based $2.05 \text{ V} \pm 0.135 \text{ V}$ supply threshold with $160 \text{ mV} \pm 13.35 \text{ mV}$ hysteresis over the temperature range -40°C to 120°C . It generates an active-low reset pulse larger than $360 \mu\text{s}$ while consuming only $7.5 \mu\text{A}$ and $360 \times 440 \mu\text{m}^2$ silicon area.

The six vector modulators embedded on-chip are controlled by the voltage generated by twelve 10-b digital-to-analog converters (DACs), namely, $vm_ctr[12:1]$. For the case at hand, the DAC IP block provided by IHP GmbH is used. The two least significant input bits are tied to a low logic level so as to conform to the 8 b of the I²C slave registers. The DACs use a 2.3-V reference to generate an output in the range from 0.4 to 2.15 V. Each DAC consumes $412 \times 86 \mu\text{m}^2$ silicon area and 70, 110, and $60 \mu\text{A}$ from the reference voltage source, 2.5- and 3.3-V power supply, respectively.

The switch control block prevents the Tx and Rx channels from being simultaneously active while switching between operating modes. It generates, from one input bit, a time sequence of two enable bits, namely, Tx_Enable and Rx_enable . A circuit based on the asynchronous edge detection is used to insert a delay between the deactivation of one output signal and the activation of the other. Simulations considering supply voltages in the range of 2.2 to 3.6 V, temperatures from -40°C to 120°C , and process corners, result in delays ranging from 33.04 to 37.87 ns. This delay exceeds the switching times of the RF active blocks and it can be thus assumed as the limiting factor of the transceiver switching speed. The block occupies an area of $42 \times 54 \mu\text{m}^2$ and the dynamic power consumption switching at 2 MHz is smaller than $4 \mu\text{A}$ for a 2-pF load.

A circuit based on the Brokaw bandgap reference cell [24] provides the necessary reference voltage to the DACs. A temperature sensor is obtained by copying the internally generated proportional-to-temperature current and converting it to a voltage in a resistance. The block occupies $234 \times 229 \mu\text{m}^2$ and consumes only $5 \mu\text{A}$ from the 3.3-V power supply. The measured samples showed that a precision better than $\pm 1.45\%$

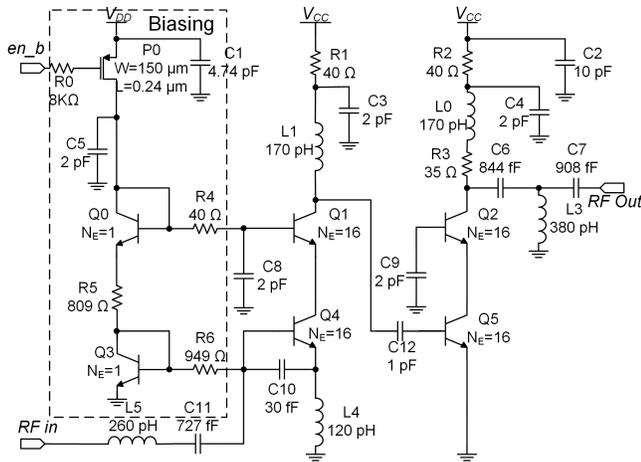


Fig. 4. Schematic of the Rx LNA. The biasing of the second stage, which is similar to that of the first one, is omitted.

can be achieved over the temperature range. The temperature sensor has a linear output dependence on temperature ranging from 0.78 to 1.3 V, or 3.25 mV/K. The small offset uncertainty, caused by variations in the resistance's absolute value, can be eliminated by realizing one measurement at a known temperature.

IV. RF MMIC BLOCKS

This section describes the design of each RF building block of the proposed chip. Each block presented in this section was designed and experimentally characterized as a single die.

A. Rx Low-Noise Amplifier

As shown in Fig. 4, a two-stage cascode LNA configuration is used to achieve high gain and low noise performance. The unit emitter area for all the HBTs presented in this paper is equal to $0.42 \times 0.84 \mu\text{m}^2$ while N_E represents the number of emitters.

The LNA uses a 3.3-V supply voltage (V_{CC}), for the amplifier core while the current mirrors are biased using 2.5 V (V_{DD}). Its activation is controlled by a dedicated control signal referred to as en_b . Ceasing the bias current will be used as a disabling method for all RF blocks, and their stages, herein reported. In some samples, a breakdown occurred because the LNA deactivation generates a peak V_{CE} in Q3 approximately 0.5 V higher than V_{BCEO} , which is equal to 2.3 V. This problem is limited to the LNA because the other RF blocks operate with 2.5-V supply. In future works, it is suggested to decrease the supply voltage available to the LNA, thereby avoiding breakdown and improving the power consumption. Another possibility is to bias the block with a fixed current rather than a fixed voltage and to allow a small standby current when the block is not used.

RF noise performance was optimized considering the optimum current density for minimum NF and selecting the number of emitter fingers equal to 16, such that an optimum noise source with a real part near 50Ω is obtained. The real part of the input impedance is modified by including

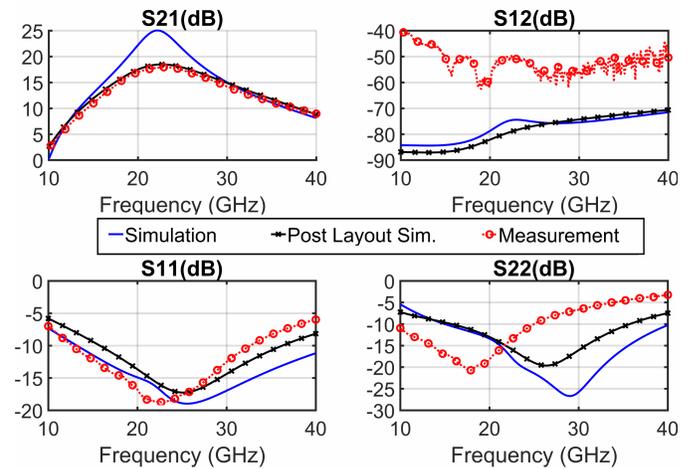


Fig. 5. Simulated and measured S-parameters of the Rx LNA.

a degeneration inductor $L4$ at the emitter of the transistor $Q4$ in the first cascode stage. The input matching network is comprised of $L5$ and $C10$, while $C11$ decouples dc. Output matching was achieved through a T-network consisting of $C6$, $L3$, and $C7$. $L1$ is the inductive load of the first stage. The second stage load is comprised of $R3$ and $L0$. $R1$ – $C3$ and $R2$ – $C4$ form low-pass filters to avoid coupling of the RF signal from other blocks through the supply voltage. RC filters were preferred over their LC counterparts as they occupy a smaller area while their loss provides a simple solution to improving the stability below the frequency range of operation.

The LNA block occupies $275 \times 420 \mu\text{m}^2$ and drains 1.8 and 15.6 mA from 2.5 to 3.3 V power supplies, respectively. The measured S-parameters are shown in Fig. 5 together with the simulated results and postlayout simulation. Measured return losses (RLs) are above 17 dB in the whole bandwidth of interest. There is a good agreement of the simulated S_{11} whereas the measured S_{22} is significantly downshifted in frequency. The measured device gain is equal to 17 dB at the center band frequency and it remains constant in the operating band. Through post layout simulations it was verified that the significant gain reduction, with respect to the simulated behavior, is due to three main reasons. First, the design kit version employed for the simulations did not model correctly the parasitic capacitances of the HBT transistors used for the LNA design. Updating the design kit results in a shift upward of the frequency of maximum gain and a small gain reduction. Second, the inductors $L1$ and $L4$ were placed physically close to each other. Mutual coupling results in negative feedback, reducing the gain of the first stage. Third, the design kit models the capacitors to be ideal. Including the interconnections in the simulations reduced the gain and shifted the MG frequency downward. The ground inductance also was identified as a cause of the gain reduction, although its impact is smaller than the reason mentioned before. As can be observed in Fig. 5, the postlayout simulations, performed using the newest version of the design kit and full-wave analysis of the layout, show, in particular for the gain, a good agreement with the measurements.

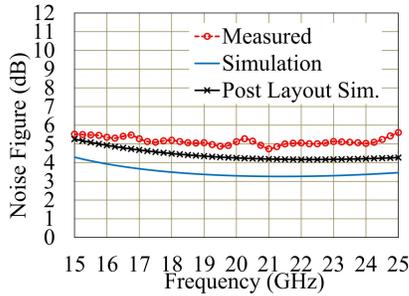


Fig. 6. Simulated and measured NF for the Rx LNA.

Fig. 6 shows the simulated and measured NF including pads. The simulated device NF is equal to 3.3 dB, whereas the measured NF, due to the gain reduction, especially of the first stage, and increased losses are equal 5 dB. In this case, the postlayout simulations result in 4.2-dB NF. Linearity simulations indicated an input referred 1-dB compression point (IP1dB) of -26.2 dBm.

B. Rx Vector Modulator

Analog reflection-type passive vector modulators [25] were used in all RF branches due to the implementable granularity of the constellation, reduced size, and zero power consumption. The granularity of the vector modulation constellation, which allows higher accuracy in setting the array elements amplitude and phase, is only limited by the control voltage step of the driving DAC. In addition, reflection-type vector modulators provide excellent linearity. One concern regarding this topology is the influence of process and temperature variations on the active loads. In this IC, the temperature sensor output can be used to correct amplitude and phase drift phenomena. The influence of process variations can be mitigated through the system calibration at the active antenna array.

In the chosen vector modulator topology, depicted in Fig. 7(a), one hybrid coupler is used at the input port to achieve signals in quadrature (I/Q). In each branch, one bi-phase modulator modifies the transmission coefficient ideally along the real axis. The signals of both I/Q branches are collected at the output by a WPC. The summation in quadrature allows four-quadrant coverage of the transmission coefficient Cartesian plane, hence full control of phase and attenuation. The 90° hybrid is realized as a spiral directional coupler [26], resulting in a reduced circuit area. Over the Rx bandwidth, its simulations indicated amplitude and phase errors smaller than 0.8 dB and 1.5° , respectively. The intrinsic loss (IL), i.e., $1 - |S_{21}|^2 - |S_{31}|^2$, is smaller than 0.4 dB. Isolation and RL are higher than 23 dB. The WPC is realized with lumped elements as reported in [17]. Its IL remains below 0.4 dB, while the RL and isolation are above 14 and 10 dB, respectively. A bi-phase modulator, realized using voltage-controlled resistive terminations with cold nMOS ($V_{DS} = 0$ V) transistors as shown in Fig. 7(b), is added to each branch of the quadrature hybrid. Assuming 90° phase shift between the two branches of the hybrid, the reflected signals at the mismatched variable

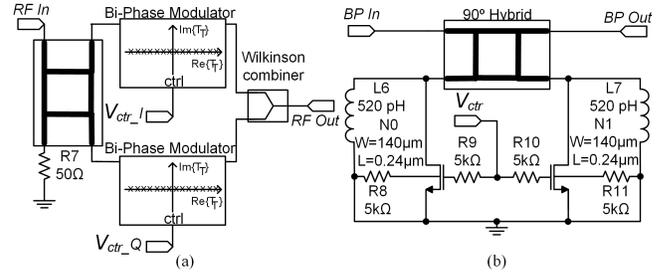


Fig. 7. Schematic of (a) Rx vector modulator and (b) bi-phase modulator.

terminations add constructively at the output and destructively at the input. The transistors $N0$ and $N1$ were dimensioned considering the DAC's voltage output range and the tradeoffs involved in the constellation quality, as discussed in [27]. $R9$ and $R10$ ensure, at high frequencies, the series connection of the drain–gate and gate–source capacitances, thus reducing the total capacitance seen at the drain of the transistors. $R8$ and $R11$ implement a floating body structure [28] to increase the power handling capability and to reduce parasitics, whereas the inductors $L6$ and $L7$ are designed to cancel the imaginary part of the variable termination around 20 GHz.

The vector modulator occupies $440 \times 458 \mu\text{m}^2$ silicon area. Fig. 8(a) shows the measured static constellation at 20.35 GHz varying the two control voltages from 0.3 to 2.3 V with 0.2-V steps. As can be observed, the four quadrants coverage is successfully achieved, although the constellation shape is rectangular, instead of square, and is not centered. The first deformation indicates an amplitude imbalance between the hybrids' quadrature ports. The second is the consequence of a relatively high ground inductance. At the center frequency, the maximum gain (MG) equals -7.54 dB, the highest attenuation (MATT) equals -26.59 dB, and the maximum achievable gain for all phases (MGAP) is -14.76 dB. Fig. 8(b)–(d) shows the S-parameters measured versus frequency corresponding to MG, MATT, and MGAP configurations, respectively. The transmission coefficient varies strongly with frequency and differently for each gain setting. Therefore, the narrowband characteristic of this vector modulator design is expected to increase the root-mean-square (RMS) gain and phase errors of the MMIC in Rx mode.

C. Tx Gain Block

The schematic of the Tx gain block amplifier is shown in Fig. 9. To simultaneously achieve high gain and the output power level required at the input of the PA, the amplifier is composed of two cascode stages with inductive loads, $L8$ and $L9$. $L10$, $C18$, and $C19$ ensure input and output matching to 50Ω , while $C20$ is added for dc decoupling. $C22$ and $C21$ implement an interstage power matching. $R13$ – $C14$ and $R14$ – $C15$ are low-pass filters suppressing interference from other blocks through the supply.

The gain block occupies $236 \times 300 \mu\text{m}^2$ and consumes 15.3 mA from the 2.5-V supply. The simulated and the measured S-parameters can be seen from Fig. 10, while

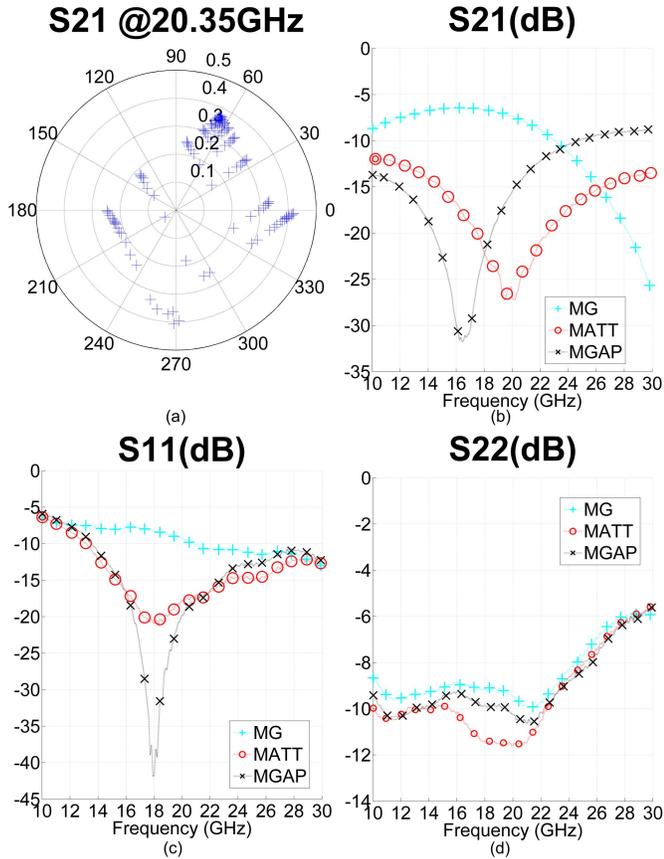


Fig. 8. Rx vector modulator measured (a) S_{21} amplitude and phase performance at 20.35 GHz varying the two control voltages from 0.3 to 2.3 V with 0.2 V steps, (b) S_{21} , (c) S_{11} , and (d) S_{22} versus frequency for MG, attenuation and possible gain for all phase configurations.

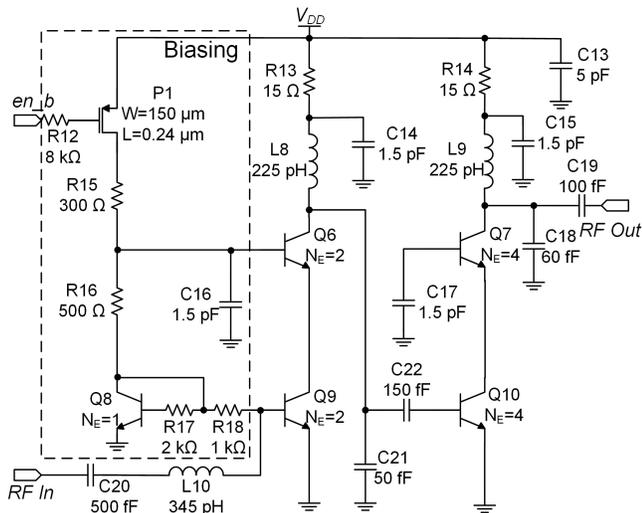


Fig. 9. Schematic of the Tx gain block. The biasing of the second stage is omitted as the same strategy as for the first stage was applied.

Fig. 11 shows linearity measurements. The S_{21} peak increased and shifted toward higher frequencies with respect to the simulations. As discussed before, the design kit did not model the HBT transistors correctly. Even so, in the

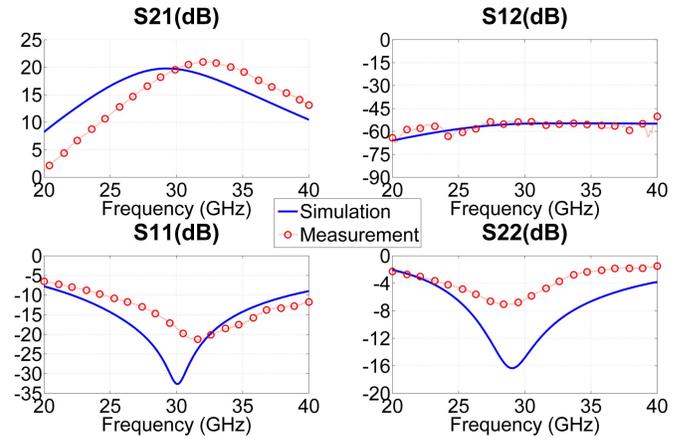


Fig. 10. Simulated and measured S-parameters of the Tx gain block.

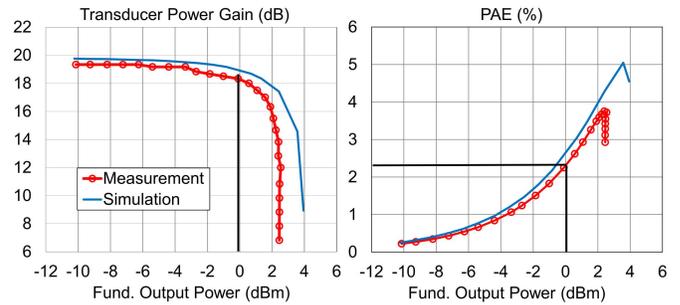


Fig. 11. Simulated and measured linearity of the Tx gain block at 30 GHz.

desired bandwidth, from 29.5 to 30.8 GHz, the gain is higher than 19.2 dB. The same frequency shift is observed also for the S_{11} , which, however, remains below -17 dB in the entire band. RLs at the output port show significant deviation with respect to the simulated response, varying between 6.3 and 5.5 dB within the range of interest. The relatively small capacitances used in the interstage and output matching networks may have decreased the circuit robustness. The linearity shows an output referred 1-dB compression point (OP1dB) of about 0 dBm at 30.15 GHz whereas the power-added efficiency (PAE) is equal to 2.3%.

D. Tx Power Amplifier

The PA of the Tx stage was designed using a class AB common-base configuration to obtain a large output voltage swing, as shown in Fig. 12. A resonant load is realized by L_{14} and C_{23} . L_{13} and C_{29} implement an open circuit at the frequencies of interest. R_{22} shifts the dc level to avoid breakdown. An L-type network matches the input to 50Ω , while a similar one at the output ensures that the optimum load is presented to the PA. C_{26} decouples the dc voltage. The current mirror Q_{11} and Q_{12} provides the bias, and the resistance R_{21} ensures similar emitter voltages for both HBTs. Considering the chosen supply voltage and class of operation, the size of Q_{12} was chosen to allow the necessary output power.

Simulated and measured S-parameter results are shown in Fig. 13. The footprint is $345 \times 360 \mu\text{m}^2$ and the block

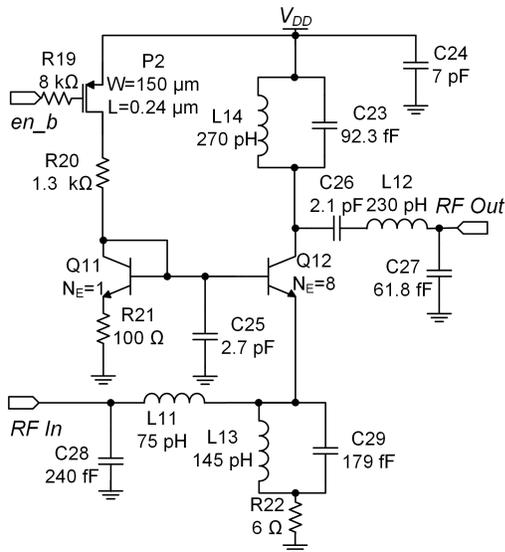


Fig. 12. Schematic of the Tx PA.

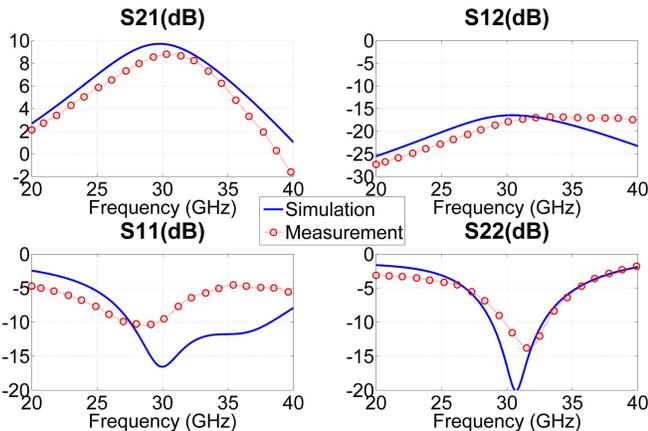


Fig. 13. Simulated and measured S-parameters of the Tx PA.

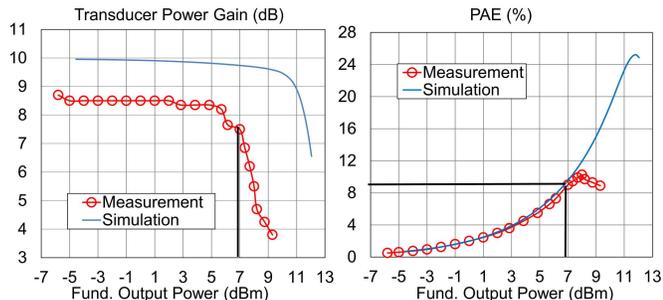


Fig. 14. Simulated and measured linearity of the Tx PA at 30 GHz.

consumes 17.1 mA from the 2.5-V supply. The gain, the input, and output RLs are better than 8.6, 8.5, and 9.2 dB across the desired bandwidth. The parasitic elements, especially due to the large C26, resulted in a strong deviation from the optimum load line, leading to reduced OP1dB and PAE, as can be seen from Fig. 14, from the expected 11 to 7 dBm and from 22% to 9% at 30 GHz, respectively.

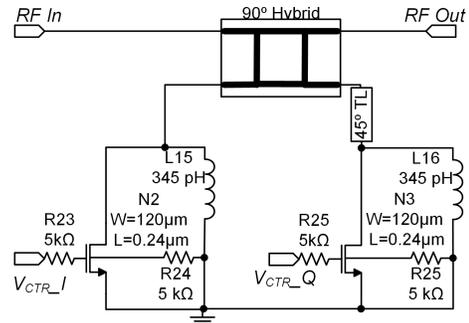


Fig. 15. Schematic of the Tx vector modulator.

E. Tx Vector Modulator

Like the Rx channel, the VM_{Tx} shown in Fig. 15 is also based on the vectorial addition of quadrature signals. However, in this case, with the intent to explore a more innovative approach, a lumped-element 45° 50- Ω transmission line (TL) is added. This line serves to provide a 90° phase shift to the signal reflected by the active load controlled by the V_{CTR_Q} voltage. The signals reflected by the two voltage controlled loads sum up in quadrature at the hybrid isolated port. A spiral directional coupler [26] was employed to implement the 90° hybrid. Over the Tx bandwidth, its simulations indicated amplitude and phase errors of 1.9 dB and 0.2° , respectively, and an IL smaller than 0.4 dB. The amplitude imbalance is partially compensated by the losses in the 45° TL. Isolation and RL are higher than 23 and 26 dB, respectively. Fig. 16(a) shows the measured static constellation at the center frequency. The total area consumption of the vector modulator is $476 \times 314 \mu m^2$. The obtained MG, MATT, and MGAP are -7.1 , -36.1 , and -12.3 dB, respectively. The constellation covers the four quadrants of the transmission coefficient Cartesian plane and is well centered. The asymmetries are mainly due to the amplitude imbalance between the two 90° hybrid channels. Fig. 16(b)–(d) shows the measured S-parameters for the mentioned configurations. Notice that at higher gains the transmission coefficient is approximately constant along the 29.5–30.8-GHz bandwidth, and varies monotonically across the measured range. As a drawback of the chosen topology, the reflected signals do not have a 180° phase difference, thus do not cancel each other and, in turn, cause low RLs dependent on the specific configuration. Even so, within the desired bandwidth, the S_{11} and S_{22} magnitudes are lower than -10.7 and -7.3 dB, respectively.

F. Rx/Tx Switch Network

The switch network is one of the key blocks of the proposed IC. Two instances of this component along with the WPC allow half-duplex operation through the reconfiguration of the chip between Tx and Rx operating mode. The switch block also provides the required isolation between the two Tx channels operating in Ka-band and one Rx front-end operating in K-band. Moreover, it also acts as a power divider by splitting the power of the common port the two Tx channels.

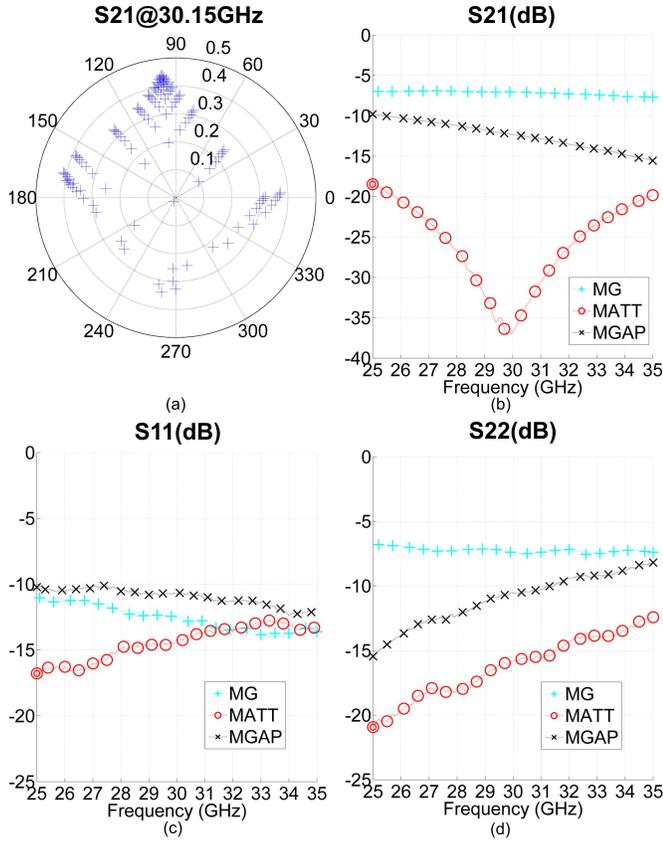


Fig. 16. Tx vector modulator measured (a) constellation at 30.15 GHz varying the two control voltages from 0.3 to 2.3 V with 0.2-V steps, (b) S_{21} , (c) S_{11} , and (d) S_{22} versus frequency for MG, attenuation and gain for all phases configurations.

The switch network has been designed including three SPST switches, one for the Rx channel and two for the Tx channels, as shown in Fig. 17. In each SPST switch, a series inductance (i.e., L_{18} , L_{16} , and L_{17}) is placed between the double shunt transistors forming π -networks to compensate their off-state capacitance. A 30-GHz WPC is embedded into the switch to equally split the Tx signal into the two channels, when in Tx mode. Additional 50- Ω TL sections providing 30° phase shift at 20 GHz, are added to each Tx branch, which will act analogously to a $\lambda/4$ transformer, when combined with the Wilkinson divider TL of length 90° at 30 GHz (60° at 20 GHz), thereby implementing an RF open in Rx mode.

The block occupies $527 \times 317 \mu\text{m}^2$ of silicon. The S-parameters of the switch network were measured showing a good agreement with the simulated results. In Rx mode, whose results are shown in Fig. 18, the switch introduces transmission losses ($-|S_{12}|$) of about 4 dB between 19.7 and 21 GHz, while the measured input reflection coefficient at the Rx port ($|S_{22}|$) remains below -8.8 dB. The reflection coefficient ($|S_{11}|$) at the common port remains below -11.8 dB. The Tx-Rx isolation is firmly above 30 dB even though, thanks to the use of self-duplexing array elements, an isolation of 10 dB would be sufficient to avoid instability due to feedback in the phased array [29].

In Tx mode, Fig. 19, the transmission losses between 29.5 and 30.8 GHz are lower than 7.4 dB including the 3 dB

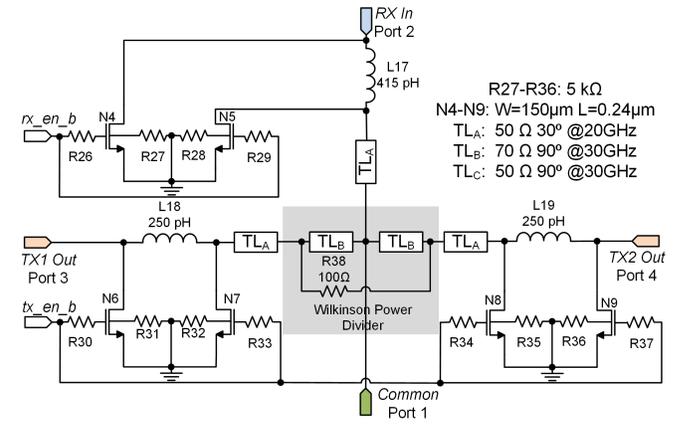


Fig. 17. Schematic of the Rx/Tx switch network.

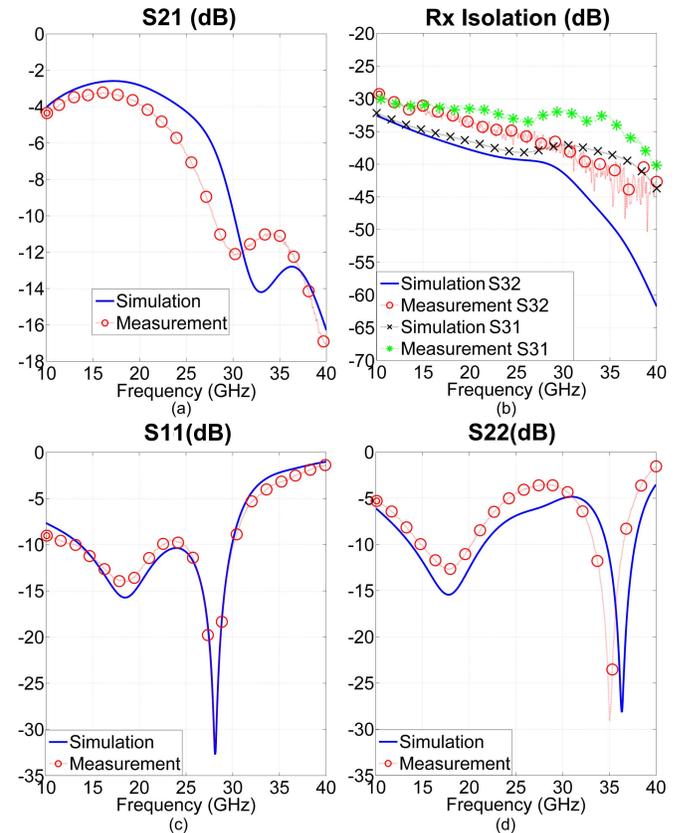


Fig. 18. Rx/Tx switch network measured and simulated results in Rx mode: (a) S_{21} , (b) Isolation, (c) S_{11} , and (d) S_{22} .

of the power splitting. The reflection coefficient at the Tx ports ($|S_{33}|$) and at the switch network input port ($|S_{11}|$) remains below -15 dB in the entire operating band. Isolation remains above 30 dB also in this operating mode. Port 4 was terminated into 50 Ω during the measurements, but due to the symmetry, results similar to port 3 are expected.

V. SYSTEM-ON-CHIP MEASUREMENTS

The proposed system-on-chip (SoC), shown in Fig. 20(a), occupies an area of $3.3 \times 3.5 \text{ mm}^2$. In Tx mode, it consumes

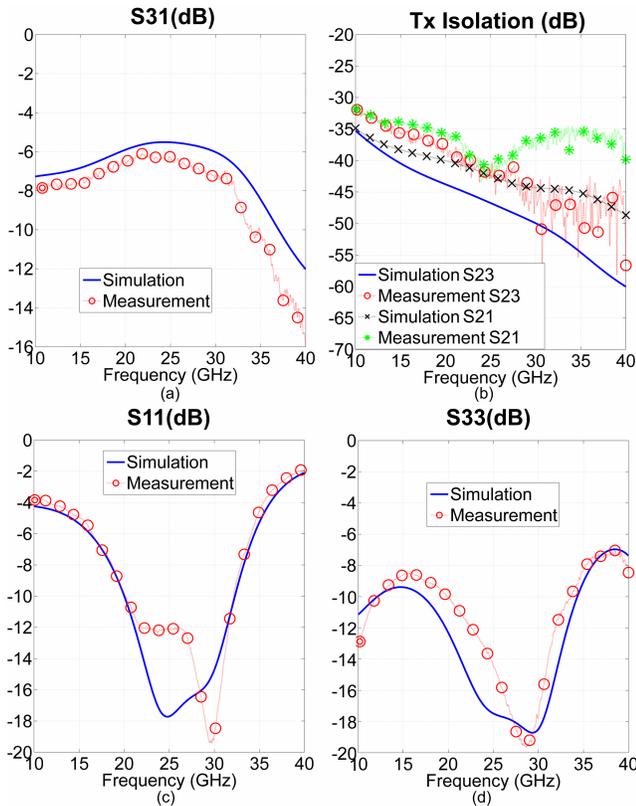


Fig. 19. Rx/Tx switch network measured and simulated results in Tx mode: (a) S_{31} , (b) Isolation, (c) S_{11} , and (d) S_{33} .

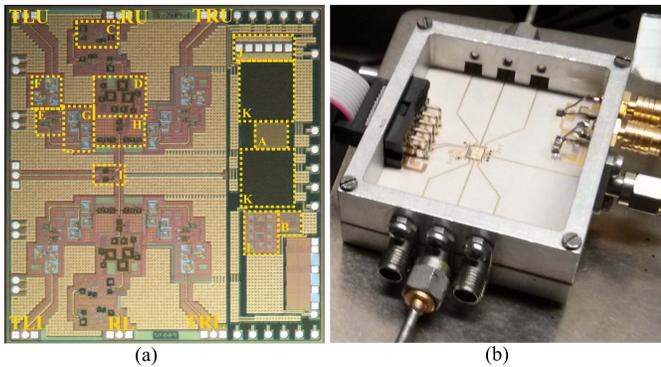


Fig. 20. (a) Micrograph of the integrated circuit, where A: I^2C slave, B: voltage reference and temperature sensor, C: LNA, D: Rx vector modulator, E: gain block, F: PA, G: Tx vector modulator, H: switch network, I: WPC, J: address pads, K: 2×6 DACs, and L: power-ON reset circuit. (b) PCB and housing for measurements.

133 and 2 mA from the 2.5- and 3.3-V supplies, respectively. In Rx mode, the power consumption changes to 7 and 68 mA, from the same supplies.

A. S-Parameters

The SoC measurement results presented here were performed using the PCB and housing shown in Fig. 20(b). The board was developed using a stackup with two dielectric layers: a Rogers RO3003, for implementing the RF 50- Ω TLs, and an FR4 layer, for power and low-frequency signals.

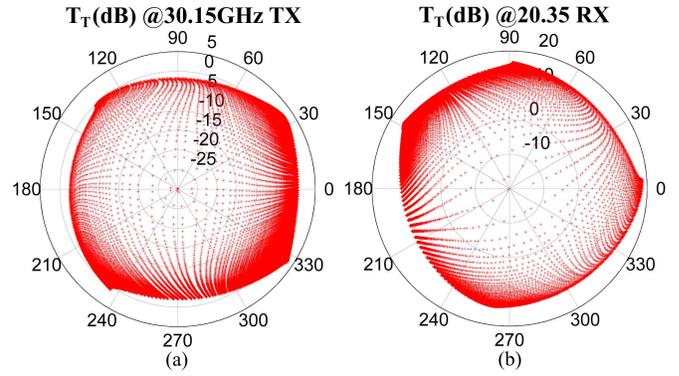


Fig. 21. (a) Transmission coefficient static constellation in Tx mode at 30.15 GHz and (b) in Rx mode at 20.35 GHz.

A cavity penetrating both materials contains the chip, reducing the length of bondwire connections while improving heat sinking. An aluminum housing was added to provide mechanical robustness and to simplify the PCB and connector integration.

The IC is supplied with 2.5 and 3.3 V. The upper and lower half of the RF function blocks and the mixed-signal blocks use both voltages, but in different domains. The precision analog block uses 3.3 V only. Thus, the total number of power domains is seven. Fifteen ground pads ensure low series impedance connection to the PCB.

Fig. 21 shows the configurable transmission coefficients constellation in Fig. 21(a) Tx mode at 30.15 GHz of the right upper Tx branch (TRU) and Fig. 21(b) in Rx mode at 20.35 GHz of the upper Rx branch (RU). For each Rx/Tx module, the S-parameters were measured in 65 536 states, using all the combinations for the two registers controlling each of the vector modulator (from 0 to 255). It is important to observe that, in order to obtain the channel gain of the MMIC as it will appear in a phased array, the gains presented herein have to be corrected by adding 6 dB to the Tx and 3 dB to the Rx modules. In Tx mode, the input power is split twice while the output of only one channel is evaluated in measuring the constellations. In the Rx mode measurements, only one channel is being fed, hence the unilateral stimulation of the WPC leads to 3 dB power dissipation in its resistance.

As observed from the static constellation plots, a good gain and coverage were obtained in the four quadrants and for both operating modes. In Tx mode, the channel MG was 9.47 dB, including the power split. With respect to the gain calculated cascading the individual blocks, 6.43 dB losses were observed. In Rx mode, the measured channel MG is equal to 21.6 dB, only 0.31 dB lower than the results expected by combining individual block measurements. This gain reduction is due to nonideal power matching between blocks and the connection losses, i.e., the losses due to the pads, the bondwires, the transitions to the 50- Ω lines, and the TL included between the PA output [block F in Fig. 20(a)] and the chip output pad. As it can be observed in Fig. 20, the physical length of the interconnection path in the Tx channels is longer than the Rx path, resulting in higher losses. Fig. 22 compares the SoC measured S_{21} in MG, MGAP, and MATT configurations,

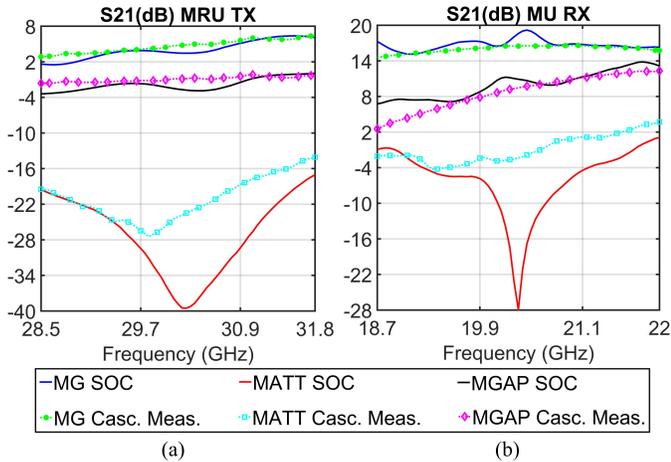


Fig. 22. SoC measurement results comparison with the cascaded measurement results for individual blocks, including full-wave simulations of the connecting intrachip TLs, of the bondwires and of the transition to the 50- Ω line in the PCB. S_{21} in (a) Tx and (b) Rx modes.

with the cascaded measured results of the individual blocks. These simulations were performed including full-wave models of the connecting intrachip TLs, of the bondwires and of the transition to the 50- Ω line in the PCB. It can be noticed that the MG and MGAP simulations are in good agreement with the measured results. For the MATT configuration the differences are due to the small number of measured VM configurations, hence the MATT control voltage of the measurement does not exactly correspond to the simulated one. Nonetheless, the same tendency is observed. It can also be noticed that some ripples are present in the S_{21} of both modes. They are due to standing waves caused by the low-cost K-type connectors soldered to the test board. The limited repeatability of the soldering procedure introduced discontinuities not perfectly removable through the de-embedding procedure. It is worth noticing that in Tx mode, this resulted in a gain reduction at the center frequency, while in the Rx mode the measured gain increased with respect to the simulations. Future works should consider the measurement setup more carefully. Better connectors, shorter TLs, and ground distribution also at the top layer of the PCB would have reduced the measurement uncertainties. The increased losses discussed above reduced the OP1dB, whose value in the proposed SoC is equal to 4.19 dBm, hence about 2.81 dB lower than the value measured for the amplifier alone. The MGAP is equal to 4.62 and 13.9 dB for the Tx and Rx mode, respectively.

B. Amplitude and Phase RMS Errors

Assuming the use of the satellite Eutelsat Hot Bird 6 (13 $^\circ$), in order to fulfill simultaneously the EIRP requirements and the maximum permissible off-axis radiation in Tx, given by the standard ETSI EN 301 459, system concepts [15] using a large number of elements and applying amplitude tapering are required. Using stochastic error analysis and considering 8 dB of Gaussian ($\alpha = 2$) amplitude tapering in a 90×90 elements array, the acceptable amplitude, and phase variance to fulfill the transmission mask is 0.5 dB and 3.2 $^\circ$, respectively.

TABLE I
MEASUREMENT RESULTS FOR ALL TX AND RX BRANCHES

Figure of Merit	Transmission				Reception		Unit	
	TRU ^a	TLU ^b	TRL ^c	TLL ^d	RU ^e	RL ^f		
MG	9.47	10.36	8.04	8.10	21.60	19.43	dB	
MGAP	4.62	5.78	3.96	3.85	13.90	13.48	dB	
MATT	-32.8	-32.2	-35.1	-31.2	-25.0	-31.3	dB	
RMS Error	Gain	0.52	0.66	0.46	0.68	2.05	1.57	dB
	Phase	3.74	5.57	3.42	6.00	12.11	13.49	$^\circ$
IP1dB	1.08	0.6	2.08	3.08	-38.4	-34.7	dBm	
OP1dB	4.19	3.7	3.69	4.36	-19.6	-17.7	dBm	
P_{sat}	6.19	5.69	5.19	5.53	-16.8	-16.9	dBm	

^a Right Upper Tx ^b Left Upper Tx ^c Right Lower Tx ^d Left Lower Tx ^e Upper Rx ^f Lower Rx

Considering this scenario, an ideal constellation was created where its maximum gain equals the measured MGAP and seven lower gain levels are provided with 1-dB steps. The phase step was chosen equal to 5.625 $^\circ$, thus corresponding to a 6-b phase control and coherent with the acceptable RMS phase error. In Rx mode, mask requirements are not present, thus, the gain is equalized at MGAP while the phase step was kept the same. The register configurations required to implement these constellations with minimum static error vector magnitude were selected as shown in Fig. 23(a) and (b) for Tx and Rx mode, respectively. Fig. 23(c) and (d) shows the measured transmission coefficients and their average in Tx and Rx mode, respectively. The lower gain settings have higher absolute errors, which can be noticed by the spreading of the measured values.

The obtained MG and phase RMS errors, 0.52 dB and 3.74 $^\circ$, are slightly above the necessary values for the proposed transmission scenario. A similar issue can be found in reception where the amplitude and phase RMS errors are equal to 2.05 dB and 12.11 $^\circ$, respectively. As expected, the narrowband characteristic of the VM_{Rx} affected these figures of merit. This block should be redesigned in the future versions.

The results obtained for all Tx and Rx paths are shown in Table I. The authors believe that the result variations between modules are more related to the measurement setup than to the SoC itself. The layout is very symmetric and the results could not be correlated with distance to supply pads or to the DACs. As discussed before, the inaccuracy in soldering the K-connectors employed to feed the test board is another source of error.

C. Linearity

Fig. 24(a) and (b) shows the channel linearity results for the TRU and the RU branches, respectively. The TX path is able to output 4.32 ± 0.49 dBm along the desired bandwidth at the 1-dB compression point with $2.91 \pm 0.42\%$ PAE, as shown in Fig. 24(c). The PAE per channel was calculated by considering the input and output power in each channel, and 1/4 of the total dc power consumption. In the Rx branch, we observe that the IP1dB is -37.18 ± 0.66 dBm.

The NF, shown in Fig. 24(d), was measured by splitting the signal coming from the noise source using a power divider

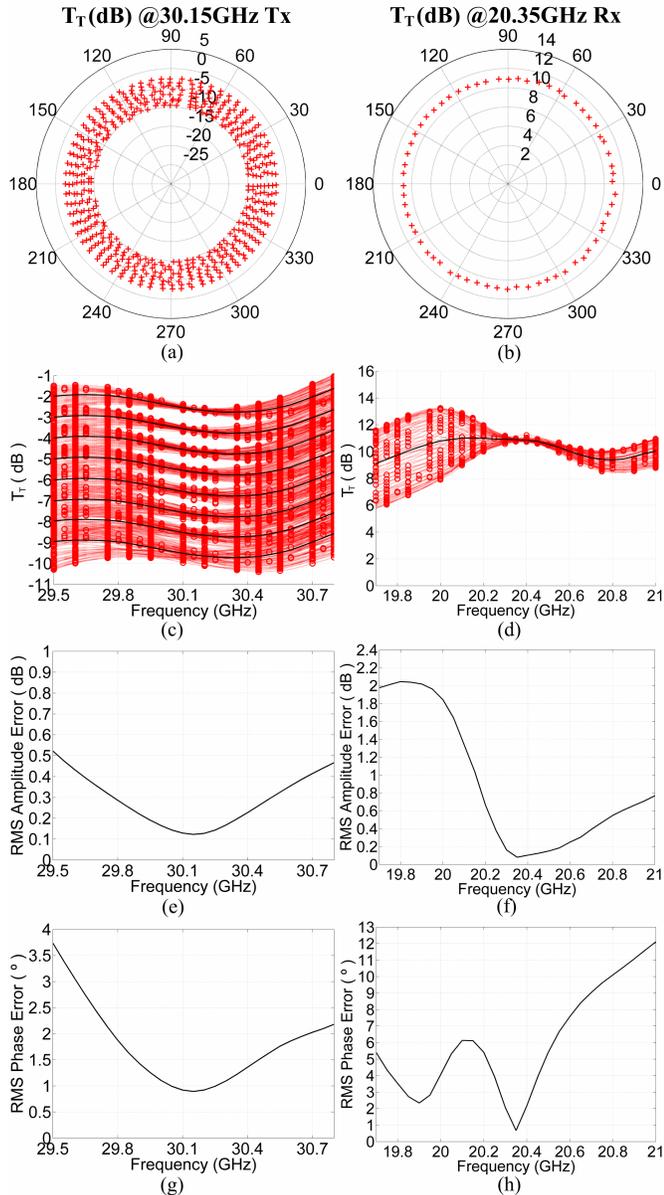


Fig. 23. Measured transmission coefficient RMS results. Constellation in (a) Tx and (b) Rx modes. Transmission coefficient amplitude in (c) Tx and (d) Rx (red dashed lines with circle markers) with average for each gain configuration (continuous black line). RMS amplitude error in (e) Tx and (f) Rx. RMS phase error in (g) Tx and (h) Rx modes.

and feeding it into each Rx channel. The combined output was measured. The vector modulator must ensure that the outputs are recombined in phase. Thereby, the same high gain configuration was set for both Rx paths.

The NF agrees with the measurements for a single LNA block, around 5 dB within the desired bandwidth.

D. Interchannel Coupling

The coupling from the Rx input to the Tx output in both operation modes is reported in Fig. 25(a). Isolations above 23.4 dB were obtained within the Tx bandwidth. Along the measurements depicted in Fig. 25(b), the IC was configured to Tx mode. The amount of power leaking from the distribution

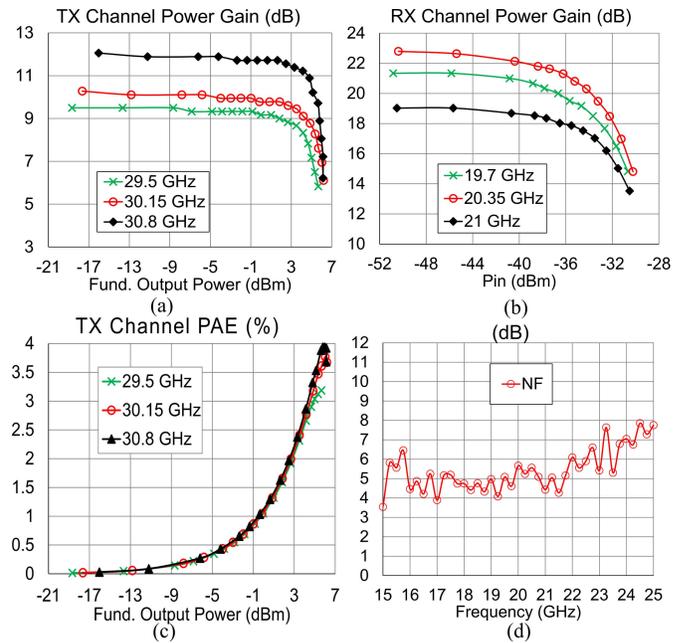


Fig. 24. (a) Channel power gain in Tx and (b) Rx modes. (c) Channel PAE in Tx and (d) NF at 20.35 GHz in Rx mode.

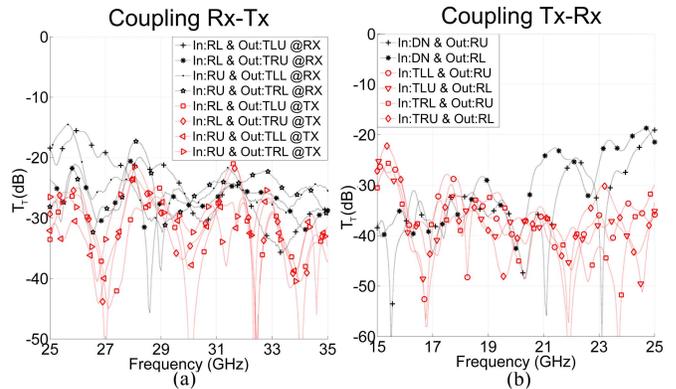


Fig. 25. Coupling between (a) Rx-Tx and (b) Tx-Rx.

network and from the port connected to the Tx antenna, used now as input, to the port connected to the Rx antenna, used now as output, is shown. Isolations higher than 19 and 24.7 dB were obtained within the entire measured and Rx bandwidth, respectively.

Based on the isolation results of the Rx/Tx switch network block, i.e., above 30 dB, a higher isolation would be expected between Rx-Tx and Tx-Rx, especially in the second case where no amplification is present in the signal path. Simulations and measurements indicated that the reverse transmission, as well as the forward transmission when the standing alone blocks are deactivated, are very low, remaining below -40 dB, -50 dB, and -16 dB for the LNA, GB, and PA, respectively. The authors believe that the coupling occurs through the ground, in the chip as well as in the measurement setup. This suspicion is reinforced by the isolation measurements performed without supply voltage, which result in isolations as low as 28 and 22.6 dB for the Rx-Tx and the Tx-Rx,

TABLE II
PERFORMANCE COMPARISON SUMMARY

Figure of Merit	This work (Tx)	This work (Rx)	[14] 2016	[18] 2009	[30] 2008	[31] 2010	[8] ^a 2008	[12] 2016	[13] 2016	
Technology	0.25 μm BiCMOS		0.13 μm BiCMOS	0.13 μm BiCMOS	0.18 μm BiCMOS	0.18 μm BiCMOS	0.12 μm BiCMOS	BiCMOS	BiCMOS	
Operating band (GHz)	29.5 – 30.8	19.7 – 21	30-40	34 – 39	6 – 18	13 – 15	35	27.5 – 30.0	17.7 – 20.2	
Functions	Half duplex Tx/Rx		Tx/Rx on the same band	Tx/Rx on the same band	Rx	Rx	Rx	Tx	Rx	
# of channels	4	2	1	4	8	2	1	8	8	
Phase shifter topology	reflection-type vector modulator		Switched LC	Switched LC	I/Q Active VM	I/Q Active VM	Switched LC	-	-	
Phase bits	8		5	5	4	4	4	5	5	
On-chip Power combining	1:6 switching/combining network		-	1:4 Wilkinson	1:8 active adder amplifiers	1:2 differential active combiner	-	1:8 with temperature compensation		
Channel Gain (dB)	9.47	21.6	Tx 14 Rx 17	Tx 0 Rx -2.5	24.5	6	11	22	22	
NF (dB)	-	5	8.4 (simul.)	9	4.2	10	3.4	-	3.4	
Rx IP1dB (dBm)	-	-33.86	-17	-16	-33 (IIP3)	-14.3	-28	-	-	
Tx OP1dB (dBm)	4.19	-	20.5	4.7	-	-	-	12	-	
Power consumption (W)	0.34	0.24	Tx 0.53 Rx 1.59	Tx 0.17 Rx 0.14	0.56	1.82	0.11	0.9	0.3	
Area (mm ²)	3.3 \times 3.5		3.2 \times 2.2	2 \times 2.02	2.2 \times 2.45	2.4 \times 4.3	0.85 \times 0.35	6 \times 6 (QFN)	7 \times 7 (QFN)	
RMS Error	Phase (°)	3.74	12.11	Tx 3.7 Rx 4	12	5.7	12	4	5	5
	Gain (dB)	0.52	2.05	Tx 0.55 Rx 0.6	0.5	0.9	1.5	-	0.5	0.25

^a Single-ended implementation

respectively. That is a drawback of single-ended topologies, which could be improved by a more careful design of the test boards and by inserting more interconnections between different ground plane sections. Nevertheless, coupling signals are not critical for the proposed application that is half duplex. Besides that, the self-diplexing antennas [10] ensure the closed loop gain below a unity in full-duplex applications [29].

E. Comparison With the Literature

Table II compares the key performance parameters of the proposed MMIC, achieved through measurements on test boards, with similar chips operating in the Ku-, K-, and Ka-bands mainly measured on-wafer.

The performance of some key blocks of the proposed design was not optimized by the time that the chip measured in this paper was manufactured. Despite the shortcomings of the chip performance, the results show the validity of the proposed approach in view of the development of a dual-band phased array. Indeed, as Table II suggests, the key feature of the proposed SoC is the half-duplex dual-band operating mode that is enabled through the on-chip power combining/dividing switch network. This dual-band operating mode is essential for implementing shared aperture Tx/Rx K/Ka SOTM user terminals and in other dual-band phased array application having a bandwidth separation between the Rx and Tx channels of the same order of the case at hand.

Moreover, the reduced number of control and bias signals is also a fundamental advantage of the presented IC, although not listed in the comparison.

VI. CONCLUSION

In this paper, a hexa-channel chip for Rx/Tx K-/Ka-band SatCom applications is demonstrated. The proposed design is the first example of a complex SoC architecture for dual-band phased arrays, specifically addressing the needs of emerging SOTM systems at two different bands (i.e., K and Ka). The chip architecture fully exploits the capabilities of a standard 0.25- μm BiCMOS process by integrating, into the same IC, four Tx, and two Rx channels with an MSCU. The six RF channels can be controlled in amplitude and phase through an I²C serial bus protocol.

At the system level, the proposed chip enables the development of a highly integrated user terminal employing a single radiating aperture for the two bands. The chip includes a digital control unit and an integrated temperature sensor. Although the results fall short of simulations in terms of output power and NF, the results presented in this paper, obtained with the first run of the chip, confirmed the general validity of the architecture. An optimization of some blocks would align the chip performance with the state of the art for similar technologies.

It is interesting to note that a first application example of the proposed chip was already presented in [32] where its

impact at system level has been fully exploited in a small-scale dual-band TX array demonstrator. Furthermore, the proposed chip configuration can be converted into a full-duplex system by replacing the switch network with the duplexer presented in [29], which is compatible with the proposed chip both in terms of performance and size.

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REFERENCES

- [1] P. Bauhahn, C. Butter, V. Sokolov, and A. Contolatis, "30 GHz multi-bit monolithic phase shifters," in *Proc. Microw. Millimeter-Wave Monolithic Circuits*, Dallas, TX, USA, 1985, pp. 4–7.
- [2] H. Takasu, F. Sadaki, M. Kawano, and S. Kamihashi, "Ka-band low loss and high power handling GaAs PIN diode MMIC phase shifter for reflected-type phased array systems," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Anaheim, CA, USA, Jun. 1999, pp. 467–470.
- [3] R. Malmqvist, A. Ouacha, and R. Erickson, "Multi-band and reconfigurable front-ends for flexible and multi-functional RF systems," in *Proc. Asia-Pacific Microw. Conf.*, Bangkok, Thailand, 2007, pp. 1–4.
- [4] T. Lambard, O. Lafond, M. Himdi, H. Jeuland, S. Bolioli, and L. Le Coq, "Ka-band phased array antenna for high-data-rate SATCOM," *IEEE Antennas Wireless Propag. Lett.*, vol. 11, pp. 256–259, Mar. 2012.
- [5] D. Kettle, N. Roddis, and R. Sloan, "A Ka-band InP MMIC 180° phase switch," *IEEE Microw. Compon. Lett.*, vol. 15, no. 6, pp. 425–427, Jun. 2005.
- [6] Y. L. Tang, N. Wadefalk, M. A. Morgan, and S. Weinreb, "Full Ka-band high performance InP MMIC LNA module," in *IEEE MTT-S Int. Microw. Symp. Dig.*, San Francisco, CA, USA, Jun. 2006, pp. 81–84.
- [7] B. W. Min and G. M. Rebeiz, "Ka-band BiCMOS 4-bit phase shifter with integrated LNA for phased array T/R modules," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Honolulu, HI, USA, Jun. 2007, pp. 479–482.
- [8] B.-W. Min and G. M. Rebeiz, "Single-ended and differential Ka-band BiCMOS phased array front-ends," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2239–2250, Oct. 2008.
- [9] B. W. Min, M. Chang, and G. M. Rebeiz, "SiGe T/R modules for Ka-band phased arrays," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp.*, Portland, OR, USA, Oct. 2007, pp. 1–4.
- [10] A. I. Sandhu, E. Arneri, G. Amendola, L. Boccia, E. Meniconi, and V. Ziegler, "Radiating elements for shared aperture Tx/Rx phased arrays at K/Ka band," *IEEE Trans. Antennas Propag.*, vol. 64, no. 6, pp. 2270–2282, Jun. 2016.
- [11] E. Meniconi, V. Ziegler, R. Sorrentino, and T. Chaloun, "3D integration technologies for a planar dual band active array in Ka-band," in *Proc. Eur. Microw. Conf.*, Nuremberg, Germany, 2013, pp. 215–218.
- [12] *Ka-Band Silicon SATCOM TX Octal Core IC, AWMF-0113*, Anokiwave Inc., Washington, DC, USA, 2016.
- [13] *Ka-Band Silicon SATCOM RX Octal Core IC, AWMF-0112*, Anokiwave Inc., Washington, DC, USA, 2016.
- [14] C. Liu *et al.*, "A Ka-band single-chip SiGe BiCMOS phased-array transmit/receive front-end," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 11, pp. 3667–3677, Nov. 2016.
- [15] F. Tabarani, T. Chaloun, T. Purtova, M. Kaynak, and H. Schumacher, "0.25 μm BiCMOS system-on-chip with four transceivers for Ka-band active reflectarrays," in *Proc. SBMO/IEEE MTT-S Int. Microw. Optoelectronic Conf.*, Porto de Galinhas, Brazil, Nov. 2015, pp. 1–5.
- [16] T. Chaloun *et al.*, "Wide-angle scanning active transmit/receive reflectarray," *IET Microw., Antennas Propag.*, vol. 8, no. 11, pp. 811–818, Aug. 2014.
- [17] E. Abaei, H. M. Aviles, A. Shamsafar, L. Boccia, and G. Amendola, "Optimum design of a miniaturized onchip wide band power divider-combiner combined with impedance transformer," in *Proc. 9th Eur. Conf. Antennas Propag.*, Lisbon, Portugal, 2015, pp. 1–4.
- [18] D. W. Kang, J. G. Kim, B. W. Min, and G. M. Rebeiz, "Single and four-element Ka-band transmit/receive phased-array silicon RFICs with 5-bit amplitude and phase control," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3534–3543, Dec. 2009.
- [19] *Maximum Permissible Levels of Off-Axis E.I.R.P. Density From Earth Stations in Geostationary-Satellite Orbit Networks Operating in the Fixed-Satellite Service Transmitting in the 6 GHz, 13 GHz, 14 GHz and 30 GHz Frequency Bands*, document ITU Recommendation S.524, 2006.
- [20] C. McLain, L. Gonzalez, and W. Hall, "Relative performance of mobile networks in the Ku, commercial Ka and government Ka bands," in *Proc. MILCOM Military Commun. Conf.*, Baltimore, MD, USA, 2011, pp. 2081–2086.
- [21] H. Fenech, A. Tomatis, and Y. Brand, "Eutelsat views on antenna requirements," presented at the 32nd ESA (Eur. Space Agency) Antenna Workshop Antennas Space Appl. (ESTEC), Noordwijk, The Netherlands, 2010.
- [22] G. Maral and M. Bousquet, *Satellite Communications Systems: Systems, Techniques and Technology*. Chichester, U.K.: Wiley, 2011.
- [23] F. Tabarani and H. Schumacher, "BiCMOS 7.5 μA power-on reset pulse generator circuit with precise threshold level and hysteresis," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Boston, MA, USA, Oct. 2015, pp. 5–8.
- [24] A. P. Brokaw, "A simple three-terminal IC bandgap reference," *IEEE J. Solid-State Circuits*, vol. SSC-9, no. 6, pp. 388–393, Dec. 1974.
- [25] L. M. Devlin and B. J. Minnis, "A versatile vector modulator design for MMIC," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Dallas, TX, USA, Jun. 1990, pp. 519–521.
- [26] K. Shibata, K. Hatori, Y. Tokumitsu, and H. Komizo, "Microstrip spiral directional coupler," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-29, no. 7, pp. 680–689, Jul. 1981.
- [27] F. Tabarani and H. Schumacher, "0.25 μm SiGe BiCMOS 30 GHz balanced vector modulator," in *Proc. IEEE 16th Topical Meeting Silicon Monolithic Integr. Circuits RF Syst.*, Austin, TX, USA, Jan. 2016, pp. 94–96.
- [28] X. J. Li and Y. P. Zhang, "Flipping the CMOS Switch," *IEEE Microw. Mag.*, vol. 11, no. 1, pp. 86–96, Feb. 2010.
- [29] A. Shamsafar *et al.*, "A four-port SiGe BiCMOS duplexer for Ka-band SatCom on the move user terminals," *IEEE Microw. Compon. Lett.*, vol. 25, no. 11, pp. 733–735, Nov. 2015.
- [30] K. J. Koh and G. M. Rebeiz, "An X- and Ku-band 8-element phased-array receiver in 0.18- μm SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1360–1371, Jun. 2008.
- [31] D. W. Kang, K. J. Koh, and G. M. Rebeiz, "A Ku-band two-antenna four-simultaneous beams SiGe BiCMOS phased array receiver," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 4, pp. 771–780, Apr. 2010.
- [32] T. Chaloun, C. Hillebrand, C. Waldschmidt, and W. Menzel, "Active transmitarray submodule for K/Ka band SatCom applications," in *Proc. German Microw. Conf.*, Nuremberg, Germany, 2015, pp. 198–201.



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